EK-MSV1J-UG-001

MSV11-J
MOS Memory

User's Guide

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MSV11-J
MOS Memory

User's Guide

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CHAPTER 1
GENERAL DESCRIPTION AND SPECIFICATIONS

1.1 INTRODUCTION

The MSV11-J is a metal oxide semiconductor, random access memory. It uses error detection and correction (ECC), a control and status register (CSR) to store status and error information, and has starting addresses on 8 kW boundaries. The board can be configured half or fully populated with 256K dynamic RAMs. Maximum memory capacity is 2 Mb.

The memory is designed for Q-bus systems and supports the private memory interconnect (PMI) protocol of the KDJ11-B processor. The PMI bus is specifically designed for and used in the PDP-11/83 Q-bus System and the PDP-11/84 UNIBUS System.

A PDP-11/83 Q-bus system uses the KDJ11-B CPU module, one or more MSV11-J memory modules and a selection of Q-bus compatible devices. Data transfers between the KDJ11-B CPU and MSV11-J memory use the PMI protocol. All other communications, whether originated by the CPU or other bus master, occur via Q-bus protocol (Figure 1-1).

NOTE: The location of the MSV11-J in the PDP-11/83 backplane determines the protocol used between the KDJ11-B and the MSV11-J. For PMI protocol, the MSV11-Js must be located immediately in front (lower slot number) of the CPU; otherwise the memory and CPU communicate with the Q-bus protocol. There should be no open slot between memory and the CPU.

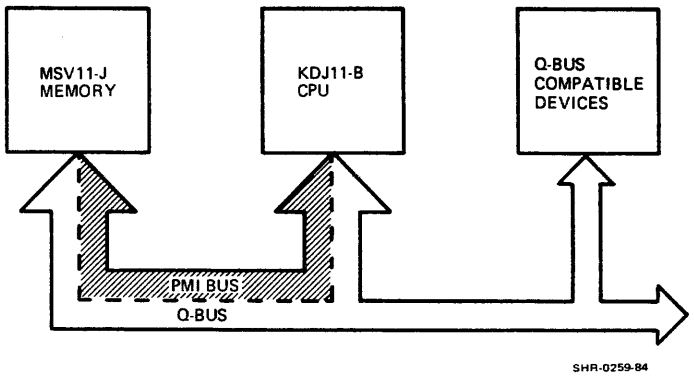


Figure 1-1 Q-Bus/PMI Bus Interface

A PDP-11/84 UNIBUS system uses the KDJ11-B CPU module, one or two MSV11-J memory modules, the KTJ11-B UNIBUS adapter (UBA) module, and a selection of UNIBUS compatible devices. The KDJ11-B, MSV11-J, and KTJ11-B modules communicate via PMI protocol. All communication between UNIBUS devices and the KTJ11-B occur via UNIBUS protocol. The KTJ11-B provides the appropriate interface between PMI and UNIBUS protocols (Figure 1-2).

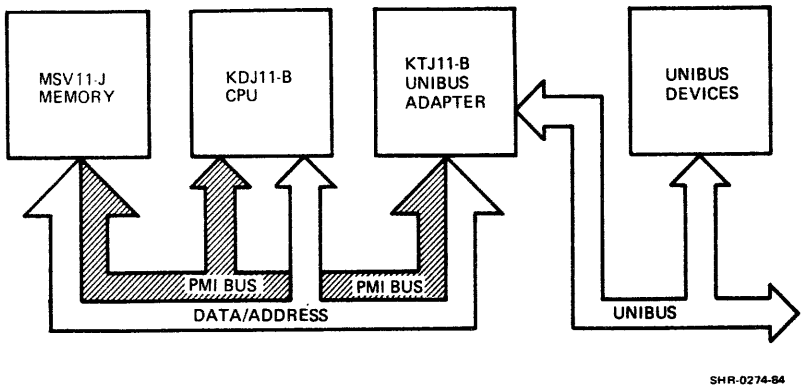


Figure 1-2 UNIBUS/PMI Bus Interface

The MSV11-J memory provides the following features.

- Starting addresses on 8 kW boundaries
- Can be half or fully populated
- Executes normal Q-bus protocol and the faster PMI protocol. Q-bus protocol is possible only with the MSV11-JD and MSV11-JE variations.
- Uses two gate arrays (VLSI technology)
- Uses advanced Schottky TTL logic
- Battery backup can be configured on board
- Green LED on module to indicate the presence of +5 volts (+5 VBB when configured for battery backup)
- On-board refresh of RAMs is transparent to CPU
- Compatible with 18- or 22-bit address backplane
- Error correction logic (ECC) to detect and correct single-bit errors and to detect double-bit errors
- Red LED on module to indicate detection of an uncorrectable error
- Contains control and status register which can be assigned one of 16 addresses
- Error correction code (ECC) operation can be controlled via CSR
- CSR operating modes facilitate diagnostic testing
- Memory compatible with Q-CD backplanes (not compatible with Q-Q backplanes)

NOTE: Insertion of the MSV11-J in a Q-Q backplane may damage other components or the memory itself. The PMI bussing on the MSV11-J's CD connectors is not compatible with the +12 V bussing on the Q-Q backplane.

1.2 DESCRIPTION

The MSV11-J is an LSI-11 Q-bus quad-height module. It uses error correction (ECC) for increased reliability and is available in the following configurations.

Option Number	Module Designation	Description
MSV11-JB	M8637-B	1 Mb ECC using 256K dynamic RAMs-PDP-11/84 ONLY
MSV11-JC	M8637-C	2 Mb ECC using 256K dynamic RAMs-PDP-11/84 ONLY
MSV11-JD	M8637-D	1 Mb ECC using 256K dynamic RAMs-PDP-11/84 or PDP-11/83
MSV11-JE	M8637-E	2 Mb ECC using 256K dynamic RAMs-PDP-11/84 or PDP-11/83

NOTE: Modules designated MSV11-JB and MSV11-JC may be used in the PDP-11/84 (UNIBUS) system only. Modules designated MSV11-JD and MSV11-JE may be used in both the PDP-11/84 and PDP-11/83 (Q-bus) systems.

The memory starting address can be set at any 8 kW boundary within the 2048 kW extended address space. (The extended address space contains 22 address lines.)

1.2.1 Error Correction

The MSV11-J contains ECC logic which detects and corrects single-bit errors and detects double-bit errors. Detecting and correcting single-bit errors is transparent to the master device accessing the memory.

1.2.2 Battery Backup

MOS storage devices are volatile (data is not retained when power is lost). Therefore, during an ac power failure, dc power is available to MOS memory for a limited time only. The MSV11-J memory module has inputs for two sources of +5 V power. These inputs are designated +5 VBB and +5 V. The +5 VBB module input can be connected to a battery backed-up power system; the +5 V input is not battery supported. In battery support mode, power is used only to refresh the MOS storage array so that battery backup time, and therefore data retention time, is maximized. A green LED on the module stays on as long as +5 VBB is available. Modules are shipped in a non-battery backed-up configuration; the module needs a jumper change to configure it for battery backed up applications.

The PDP-11/84 system can be shipped in a battery backup system configuration or in a non-battery backup system configuration. In a battery backup system configuration, the memory is tied to the battery backup supply through the backplane and power connector. Therefore, the MSV11-J modules should not be configured for battery backup mode in either of the above mentioned system configurations.

1.2.3 ECC Initialization

The MSV11-J performs an error correction initialize (ECC INIT) operation after the power-up (+5 BBU power up in battery backed up systems). For an ECC INIT operation, a pattern is written into all memory locations in the MOS storage array. All MOS RAMs on the module are written sequentially during initialization. The circuitry senses the presence of 5 VBB and DCOK before starting the initialization sequence. Signal BPOK is deasserted by memory while ECC INIT is in progress.

1.2.4 Control and Status Register (CSR)

The control and status register in the MSV11-J allows program control of certain ECC functions, and stores diagnostic information if an error occurs. The CSR has its own address in the I/O peripheral page, and can be read or written into by any device designated as bus master.

1.2.5 Bus Cycles

The MSV11-J supports the following Q-bus and PMI bus cycles (Tables 1-1 and 1-2). These bus cycles, executed by bus master devices, transfer 16-bit words or 8-bit bytes to or from slave devices.

Table 1-1 Q-Bus Cycle – MSV11-JD and -JE Only

Bus Cycle Mnemonic	Description	Function (with Respect to Bus Master)
DATI	Data word input	Read
DATO	Data word output	Write
DATOB	Data byte output	Write byte
DATIO	Data word input/output	Read-modify-write
DATIOB	Data word input/byte output	Read-modify-write byte
DATBI	Block mode input	Block Read
DATBO	Block mode output	Block Write

Table 1-2 PMI Bus Cycle

Bus Cycle Mnemonic	Description	Function (with Respect to Bus Master)
(P) DATI*	Data input (2 words)	Read
(P) DATBI*	Block mode input	Block mode read
(P) DATO*	Data word output	Write
(P) DATOB*	Data byte output	Write byte

* The P in parentheses preceding the cycle type denotes PMI cycle.

1.2.6 Refresh

The MSV11-J refresh circuitry guarantees that the data stored in the MOS RAMs is valid for extended periods of time. The interval between refresh cycles is set to about 14 μs to guarantee accessing all 128 rows in 2 ms (128 cycle refresh) or 256 rows in 4 ms (256 cycle refresh).

Refresh requests are initiated every 14.0 μs $\pm$ 5 percent from an asynchronous oscillator on the module. These single refresh cycles are initiated at the end of a bus memory access. If the memory does not receive a bus memory access request within 9 μs of a single refresh request, it changes that request to a double refresh request, appending two refreshes to the end of the next bus memory access. Double refresh is not valid on the MSV11-JB or MSV11-JC memories.

A refresh priority cycle is enabled if a bus memory access has not occurred within two refresh periods (i.e., 28 μs) and the refresh request cycles have not been peformed. During a refresh priority cycle, the next memory cycle is preceded by two refresh cycles. If a memory cycle is not initiated within 3 μs of the assertion of refresh priority cycle, the refresh logic initiates its own refresh demand cycle.

1.2.7 Simplified Block Diagram Description

Figure 1-3 is a simplified block diagram of the memory. The bus interface, address gate array, data gate array, and MOS storage array are shown. The address gate array contains the ECC initialization circuitry, memory refresh circuitry, and the timing and control for PMI and Q-bus cycle types.

The data gate array contains the ECC logic, generates check bits for write cycles, and uses the check bits during read cycles to detect and correct single-bit errors and to detect double-bit errors.

The half-populated MOS storage array consists of two blocks – block 0 and block 1. The fully populated MOS storage array consists of four blocks – blocks 0, 1, 2, and 3. Each block is 22 bits wide and 256K deep (see Figure 1-4).

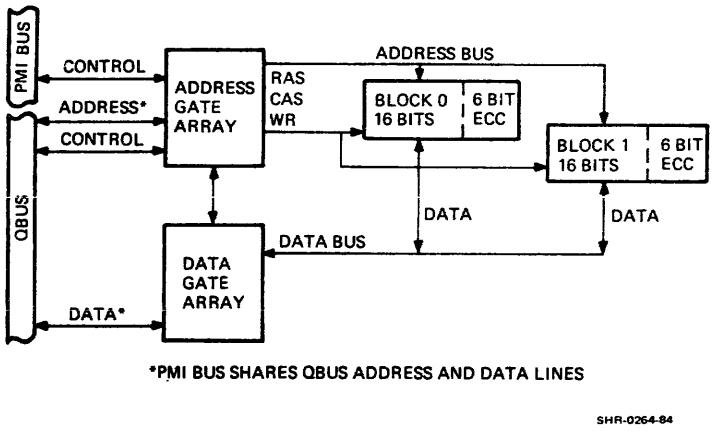


Figure 1-3 MSV11-J Simplified Block Diagram

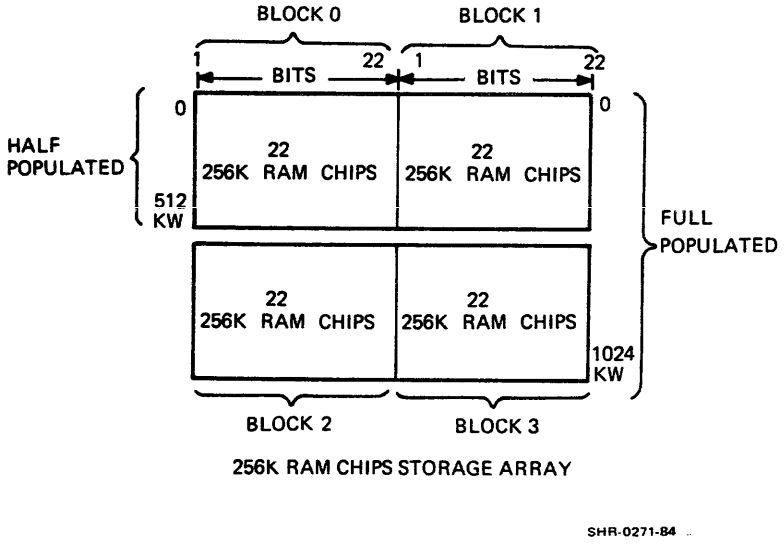


Figure 1-4 MOS Storage Array Architecture

The 22-bit words in memory consist of 16 data bits and 6 check bits. The check bits are generated by the data gate array for each 16-bit data word. Although the MSV11-J memory word is 22 bits long, the bus master transactions are 16-bit words. The 6 check bits are internal to the memory.

The control and status register (CSR) performs the following major functions.

- It disables or enables error reporting to the CPU.
- It allows diagnostic programs to be run without having the diagnostic interfere with the check bits in the protected diagnostic area.
- It disables ECC, if desired. MSV11-J detects but does not correct errors.
- It flags single- or double-bit errors. If ECC is enabled, single-bit errors are corrected.
- The address of the error is latched in the CSR unless higher priority (double-bit error) is present.
- In diagnostic mode, syndrome or check bits can be returned to the processor if desired.

1.3 Error Correction Code (ECC)

ECC is a technique used to increase reliability of MOS memory. This is done by correcting single-bit errors. The use of ECC with MOS memory requires additional logic to generate check bits used in the detection and correction process.

ECC is practical not only due to the low cost of memory and logic, but also because the predominant failure mode in dynamic RAMs is single cell failures, distributed randomly. These failures occur at a low rate and the probability of two such failures (or one such failure and a soft bit error) occurring in coincidence is extremely small.

1.3.1 Advantage of ECC

MOS RAM technology is constantly evolving and the RAM density quadruples for each new RAM introduction. Larger memory arrays make the probability of errors slightly higher even though the reliability of RAMs is improving.

Some advantages of using ECC with MOS RAM technology are:

- MOS RAMs, unlike core, are more susceptible to noisy power supplies.
- Soft errors due to inherent radiation traces (alpha particles) occasionally cause an individual bit in the RAM to lose its data. These soft errors are overwritten during the next WRITE to that location. ECC prevents a system failure until the overwriting can occur.
- Most hard errors (due to aging or premature defect of the RAM) occurring in a desired (by CPU) address cause a failed bit.

These three types of failures cause a system failure in parity memory but are transparent in ECC memory. ECC makes single-bit failure in the RAM transparent to the CPU by correcting single-bit errors "on the fly" before the CPU receives it. It thereby increases the effective MTBF (mean time between failures) of main memory. Also the memory failure rate doesn't proportionally increase as memory capacity increases.

1.3.2 ECC Operation

A check bit code is generated on each memory write cycle. This code is written into memory along with the 16-bit data word. On a memory read cycle, the check bits are read from memory along with the 16-bit data word. New check bits are generated and compared with the check bits read from memory. If the two groups of check bits are alike, no error is detected. If they are different, the difference between the two groups of check bits (syndrome bits) determines the failed bit, provided there is only one error. The ECC circuitry corrects the bit in the word and sends the word to the CPU.

In the case of a multiple error, the word is not corrected and is sent to the CPU with an asserted signal line warning the CPU that this data is invalid. This signal has the same effect as a parity flag in parity memory, at the occurrence of a single-bit error.

1.3.3 Example of ECC-Implementation

A fully populated MSV11-J is a 2 Mb memory. The memory storage consists of 22-bit words, (16 data bits plus 6 check bits) each bit position being in a different memory chip (RAM). However, the CPU reads from memory, or writes to memory, in 16-bit words.

For a write cycle (DATO function), the memory receives (from the CPU) the 16-bit word and generates the 6 check bits. This new 22-bit word is stored in the memory array.

For a read cycle (DATI function), the 22-bit word is fetched from memory and divided into two; the original 16-bit word (data) and 6 check bits. New check bits from the 16-bit data word are generated and compared with the check bits read from memory. If a single-bit error occurs, the ECC circuitry in memory corrects the data word containing the error. The corrected word is then transferred to the CPU. The data in the original memory location remains uncorrected.

For a DATOB function, only a byte is written into memory. To accomplish this function, the entire 16-bit data word and 6 check bits residing in memory must be read and checked for errors. Any single-bit error in the word is corrected. Assume, for example, that the CPU desires to write the lower byte. The new lower byte is combined with the high byte to form a new 16-bit data word. Check bits are generated on the new word and the entire word (16 data bits plus 6 check bits) is written back to memory.

The sequence of events is:

1. 22 bits read from memory.
2. Single-bit error corrected, if required.
3. New byte combined with old byte.
4. 6 check bits generated on new 16-bit word.
5. New 22-bit word written to memory.

1.4 SPECIFICATIONS

This paragraph describes the various MSV11-J specifications including access and cycle times for the Q-bus and P-bus protocol.

1.4.1 General Specifications

Height	10.436 inch quad height
Width	0.5 inch
Length	8.94 inch bottom of fingers to top of handle, extended
Etch	8 mil multilayer

User Options	Default (All Switches Off)
Starting address 8 kW boundaries	Starting address = 0
CSR address (1 of 16)	CSR = 0 (17772100)
System size Q18 or Q22	Q22

New Technologies

Drams	256K dynamic RAMs
Gate arrays Advanced Schottky TTL	F series (fast) logic

Battery Backup

5 VCC for bus support logic
5 VBB for MOS RAMs and refresh

Refresh

Interval between refresh cycles (guarantees accessing all 128 rows in 2 ms or 256 rows in 4 ms)	14.0 μs ± 5%

Error Correction Code
Detects single and double-bit errors and corrects single-bit errors

1.4.2 Environmental Specifications

Temperature

Storage Temperature Range	−40 to +66 degrees Celsius

Before operating a module which is at a temperature beyond the operating range, that module must first be brought to an environment within the operating range and then must be allowed to stabilize for a minimum of five minutes.

Operating Temperature Range	+5 to +60 degrees Celsius

De-rate the maximum operating temperature by one degree Celsius for each 1000 feet of altitude above 8000 feet.

Relative Humidity

Storage	10 to 90%, noncondensing
Operating	10 to 90%, noncondensing

Operating Airflow
When the inlet temperature is +60 degrees Celsius, adequate airflow must be provided to limit the inlet to outlet temperature rise across the module to 5 degrees Celsius. For operation below +55 degrees Celsius, airflow must be provided to limit the inlet to outlet temperature rise across the module to 10 degrees Celsius maximum.

Altitude

1. Storage
   The module will not be mechanically or electrically damaged at altitudes up to 50,000 feet (90 MM mercury).

2. Operating
   Up to 50,000 feet (90 MM mercury).

NOTE: De-rate the maximum operating temperature by one degree Celsius for each 1000 feet of altitude above 8000 feet.

1.4.3 Electrical Specifications

1.4.3.1 Power Supply Requirements – The module operates on +5 V only, with provisions made for operating in a battery backup mode for long term data retention.

MSV11-JB, JD

	Current, Amps					
	Standby		**Active**		**ECC Init**	
	Typ	**Max**	**Typ**	**Max**	**Typ**	**Max**
+5 V only	0.5	0.56	0.5	0.57	0.5	0.57
+5 V BBU	0.8	1.41	1.0	3.37	1.0	2.54
+5 V Total	1.3	1.97	1.5	3.94	1.5	3.11

MSV11-JC, JE

	Current, Amps					
	Standby		**Active**		**ECC Init**	
	Typ	**Max**	**Typ**	**Max**	**Typ**	**Max**
+5 V only	0.5	0.56	0.5	0.57	0.5	0.57
+5 V BBU	1.0	1.72	1.2	3.72	1.25	4.00
+5 V Total	1.5	2.28	1.7	4.29	1.75	4.57

The 5 VCC and 5 VBB power supplies must not exceed the range minus 1.0 V to plus 7.0 V to avoid permanent stress damage to the MOS RAMs. Operating voltage range is 5 V ± 5 percent.

1.4.4 Interface Specifications

1.4.4.1 P-Bus Interface – The memory communicates with the KDJ11-B processor via an enhanced protocol (p-protocol). Essentially, reads are two word transfers which take advantage of the KDJ11-B restart overhead to load a second 16-bit word into the cache on the CPU module. Write operations are initiated just after addresses are valid.

1.4.4.2 Q-Bus Interface – In addition to the p-protocol, the memory is compatible with the LSI-11 bus (Q-bus). All signals are one bus load.

NOTE: MSV11-JB and MSV11-JC cannot perform Q-Bus protocol.

1.4.4.3 Signal AC/DC Loading –

2.5 ac loads	(1 ac load = 9.35pF)
0.5 dc loads	(1 dc load = 105 uA nominal)

1.4.5 Performance Specifications

This paragraph lists the access and cycle times for the P-bus and for the Q-bus.

NOTES:

1. *Memory performance is the time measured from the output of the bus receivers to the input of the bus drivers.*
2. *This assumes PWTSTB occurs within 145 ns of PBCYC. Longer time to PWTSTB extends cycle time an equivalent amount of time.*
3. *Correction of single errors extend the access time of PMI DATI or DATBI cycles by 116 ns maximum.*
4. *R PBCYC to T PRD STB trailing edge.*
5. *T PRD STB trailing edge to second word valid.*
6. *R PBCYC to memory BUSY de-asserted.*
7. *T PRD STB trailing edge to next T PRD STB trailing edge with minimum PBLK response from bus master (240 ns).*
8. *R DAL (address) valid to T PSSEL.*
9. *R SYNC to TRPLY with minimum time from R SYNC to RDIN/RDOUT (25 ns/50 ns).*
10. *R SYNC to memory BUSY de-asserted.*
11. *DATO (B) cycles assume 50 ns from R SYNC to RDOUT.*
12. *The first transfer in a DATBI is the same as a DATI. Subsequent word access times are measured from R DIN de-asserted to TRPLY asserted with minimum bus timing (i.e., TRPLY negated to RDIN asserted = 150 ns). DATBI access time alternates between these two values due to the two word read architecture of the memory. Even word accesses (as determined by DAL 01) have a longer access and cycle time. Subsequent odd transfers realize the faster access and cycle time.*
13. *Minimum bus timing from T RPLY de-asserted to R DOUT asserted.*

14. *R PBCYC to memory BUSY de-asserted after 8 double-word transfers (16 words transferred) assuming minimum P BLK response from master (240 ns).*

15. *R QSYNC to memory BUSY de-asserted after 16 word transfers assuming minimum TRPLY, R DIN bus master timing.*

Refresh
All access and cycle times are extended whenever a refresh conflict occurs.

Refresh Cycle Time	Maximum (ns)
Single refresh request*	538
Double refresh request*	1006
Refresh priority†	1483
Refresh demand‡	1483

1.4.5.1 P-Protocol Access and Cycle Times (All MSV11-J Variations)

Memory Performance (1)

	Access Time (ns)				Cycle Time (ns) (6)			
	Min	Typ	Max		Min	Typ	Max	
DATI (3) 1st word (no error)	390	417	444	(4)	538	568	597	
2nd word	35	58	80	(5)	–	–	–	
DATBI (3)	518	531	545	(7)	3794	4166	4539	(14)
DATO	30	38	45	(8)	538	568	597	(2)
DATOB (3)	30	38	45	(8)	746	788	829	(2)
DATI CSR access	390	417	444	(4)	538	568	597	
DATO CSR access	30	38	45	(8)	538	568	597	

* Refresh requests are added to the end of a bus memory cycle. The next bus memory cycle is postponed until this refresh cycle is completed. Double refresh is not valid on MSV11-JB and MSV11-JC.

† Refresh priority cycles precede a memory cycle and delay access and cycle times.

‡ Refresh demand cycles are self-initiated and may delay memory access and cycle times up to this length of time.

1.4.5.2 Q-Protocol Access and Cycle Times (MSV11-JD and MSV11-JE Variations Only)

Memory Performance (1)

	Access Time (ns)				Cycle Time (ns) (10)			
	Min	**Typ**	**Max**		**Min**	**Typ**	**Max**	
DATI	269	327	386	(9)	556	605	654	
DATBI								
Even	268	324	381	(12)	7261	8032	8802	(15)
Odd	212	269	325		–	–	–	
DATO (11)	88	135	182	(9)	606	655	704	
DATBO (11) (13)	88	135	182		9423	9805	10187	(15)
DATOB (11)	88	135	182	(9)	772	850	929	
DATIO (13)	269	327	384	(9)	1208	1333	1457	
DATIOB (13)	269	327	384	(9)	1415	1553	1691	
DATI CSR access	269	327	386	(9)	556	605	654	
DATO CSR Access (11)	88	135	182	(9)	606	655	704	

CHAPTER 2
DATA FLOW

2.1 INTRODUCTION

This chapter describes the basic data flow for read, write, and write byte cycles. Other bus cycle types are basically combinations of these. For example, block mode read cycles are similar to a succession of read cycles.

Each bus cycle contains an address portion and data transfer portion. The address portion of the various bus cycle types are similar in that the processor is addressing the slave device. The data transfer portion of each bus cycle type differs since the data flows in different directions for different cycle types. For example, a read cycle transfers data from memory to the processor while a write cycle transfers data from the processor to memory.

2.2 ADDRESS PORTION OF BUS CYCLE

Figure 2-1 shows the address flow portion of the bus cycle. In the PMI bus protocol, if the address specified by the processor is within the address of the memory, the memory responds with a control signal to indicate that it has been selected.

In the Q-bus protocol, if the address specified by the processor is within the address range of the memory, the memory executes the requested cycle.

The address portion of the bus cycle is initiated when the processor places a 22-bit address on the bus. The address is received and compared with the memory's starting address to determine if the addressed location resides on that memory board. Nine of the address bits specify the row address and nine specify the column address.

After the row address becomes stable, row address strobe (RAS) is asserted.

The address gate array then switches from row address to column address. After the column address becomes stable, column address strobe (CAS) is asserted. Note that the nine address lines at the output of the address gate array are multiplexed and supply the row address followed by the column address.

The RAMs have multiplexed address inputs. Eighteen address bits (9 row address and 9 column address bits) are required to supply a unique address for each memory location.

There are 22 RAMs in each data word (88 RAMs on a fully populated board). There is one RAM for each bit of the 16-bit data word and one for each of the 6 check bits.

Each set of 22 RAM chips makes up a block of memory. A fully populated board has 4 blocks or a total of 88 RAM chips (see Figure 1-4).

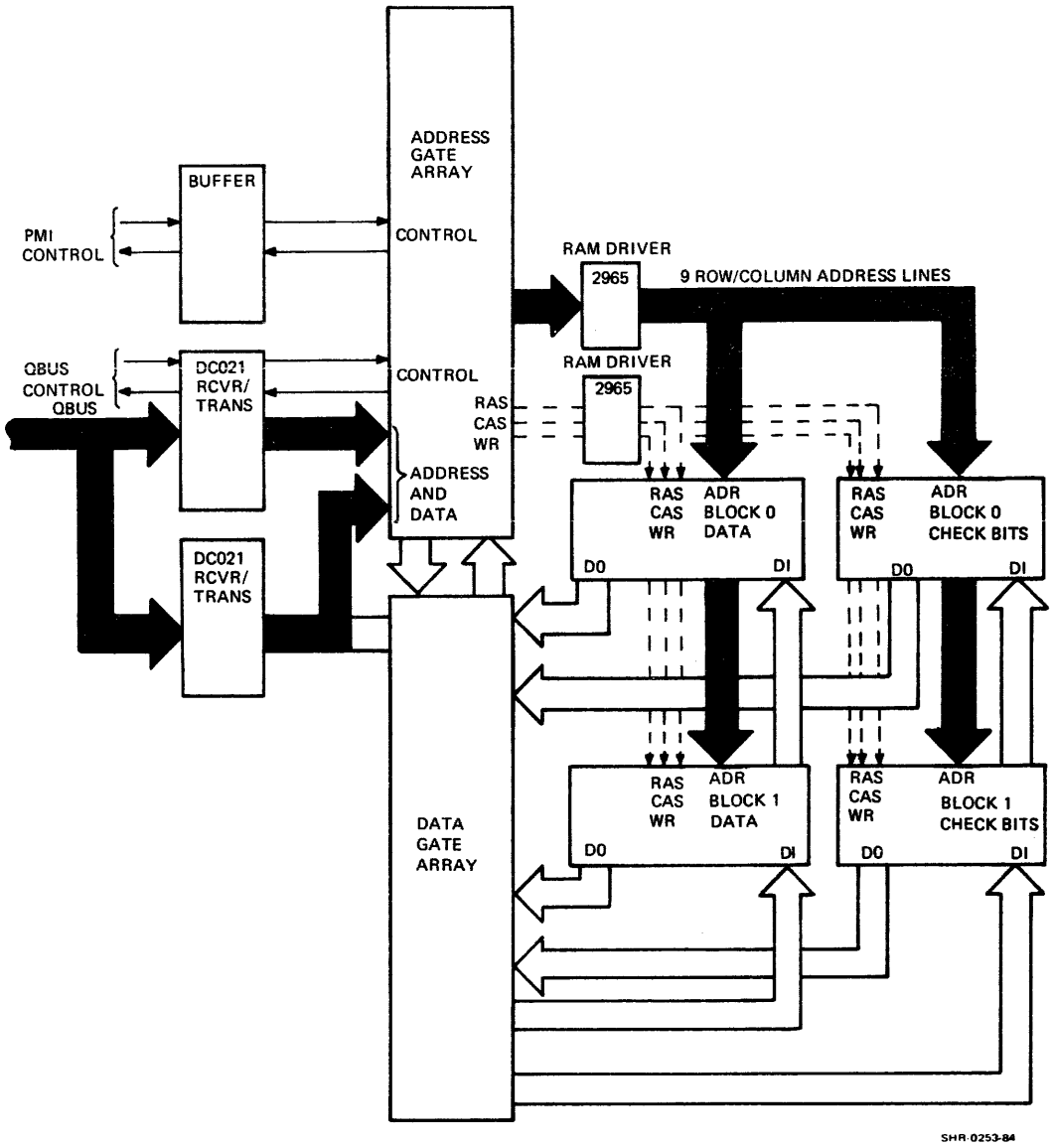


Figure 2-1 Address Flow (Read, Write, Write Byte)

The row and column address bits specify the same address in all blocks. Therefore, two additional bits are required to uniquely define one of the blocks. One bit (BDAL1) defines odd/even word selection for a read or write cycle. In other words, BDAL1 selects the left (even) block or the right (odd) block (Figure 1-4). The second bit is BDAL20 which selects the upper block or the lower block.

For a write cycle, the processor must specify which block the word is to be written to. This is accomplished by BDAL1 and BDAL20.

2.3 DATA TRANSFER PORTION OF BUS CYCLE

The following paragraphs describe the data transfer portion of the read cycle, write cycle, and write byte cycle in terms of data flow.

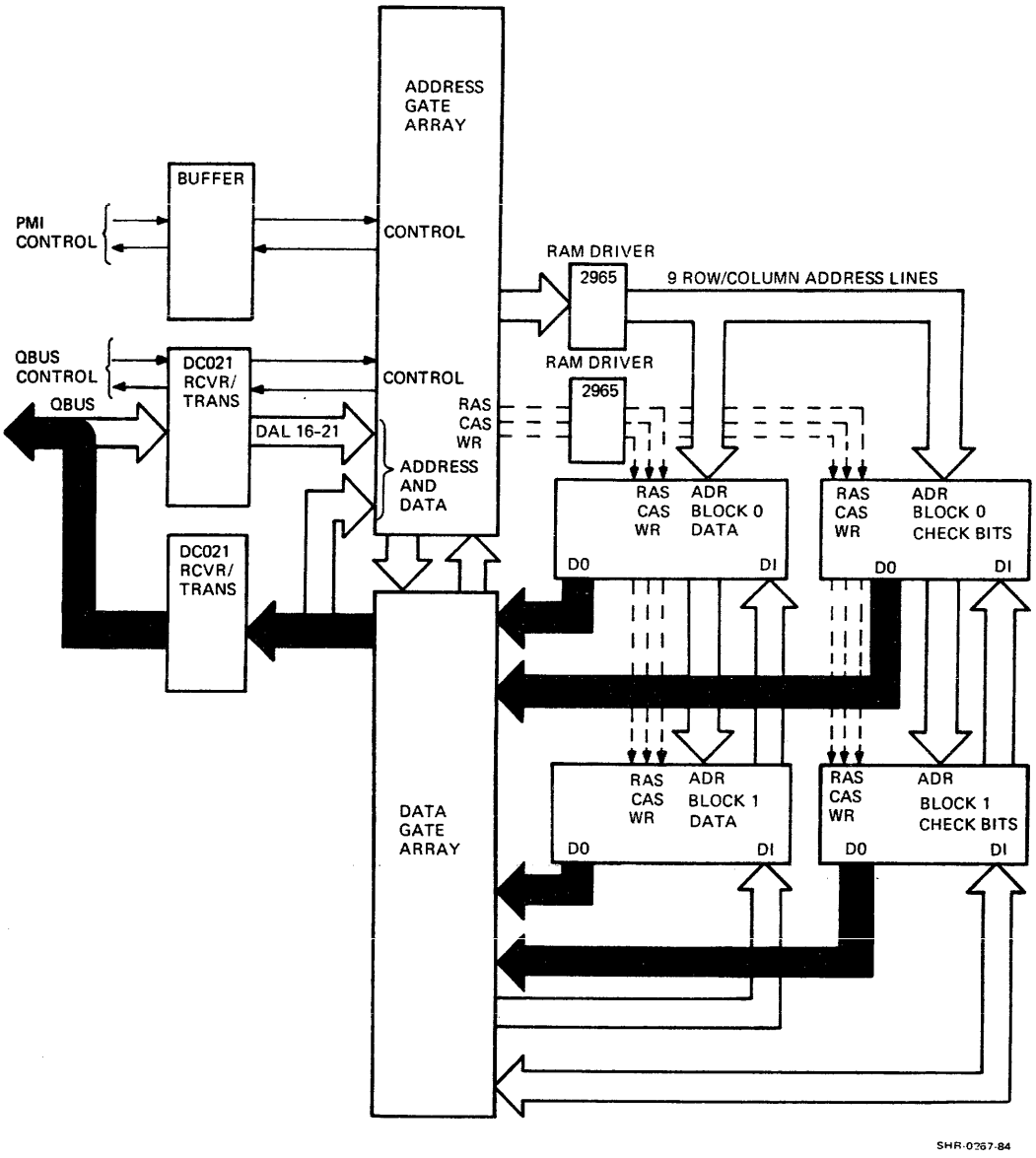


Figure 2-2 Read Cycle Data Flow

2.3.1 Read Data Transfer (Figure 2-2)

Read cycles are executed as two-word reads from two different locations – one word from block 0 and one word from block 1.

When CAS goes low, the RAM output drivers are turned on. After data becomes valid, the two 22-bit words are transferred to the data gate array and latched in this array under control of the address gate array.

For a Q-bus read cycle, the processor specifies which word is to be transferred. For a PMI-bus read cycle, the processor specifies which word is transferred to the bus first. This is accomplished by BDAL1.

If Q-bus protocol is used, only one word is placed on the bus. BDAL1 selects the word to be placed on the bus. If an error occurs in the first word, the error is corrected and no loss in access time occurs.

If PMI protocol is used, both words are placed on the bus serially. BDAL1 selects the word to be placed on the bus first. If an error occurs in the first word of the two-word read, the data is stalled while the error correction takes place. If an error occurs in the second word instead of the first word, the error is corrected with no loss of cycle time.

2.3.2 Write Data Transfer (Figure 2-3)

Write cycles are single-word writes to RAM. The processor places a 16-bit data word on the bus thus initiating the data transfer portion of this bus cycle. The data is received by two DC021 transceivers and then the data gate array. The data gate array generates 6 check bits from the 16-bit data word. The address gate array determines which block of memory is written and asserts the write signal. The 22-bit word is then written in the appropriate block.

The state of BDAL1 determines in which block of memory the word is written. If BDAL1=0, the word is written in block 0 and if BDAL1=1, the word is written in block 1.

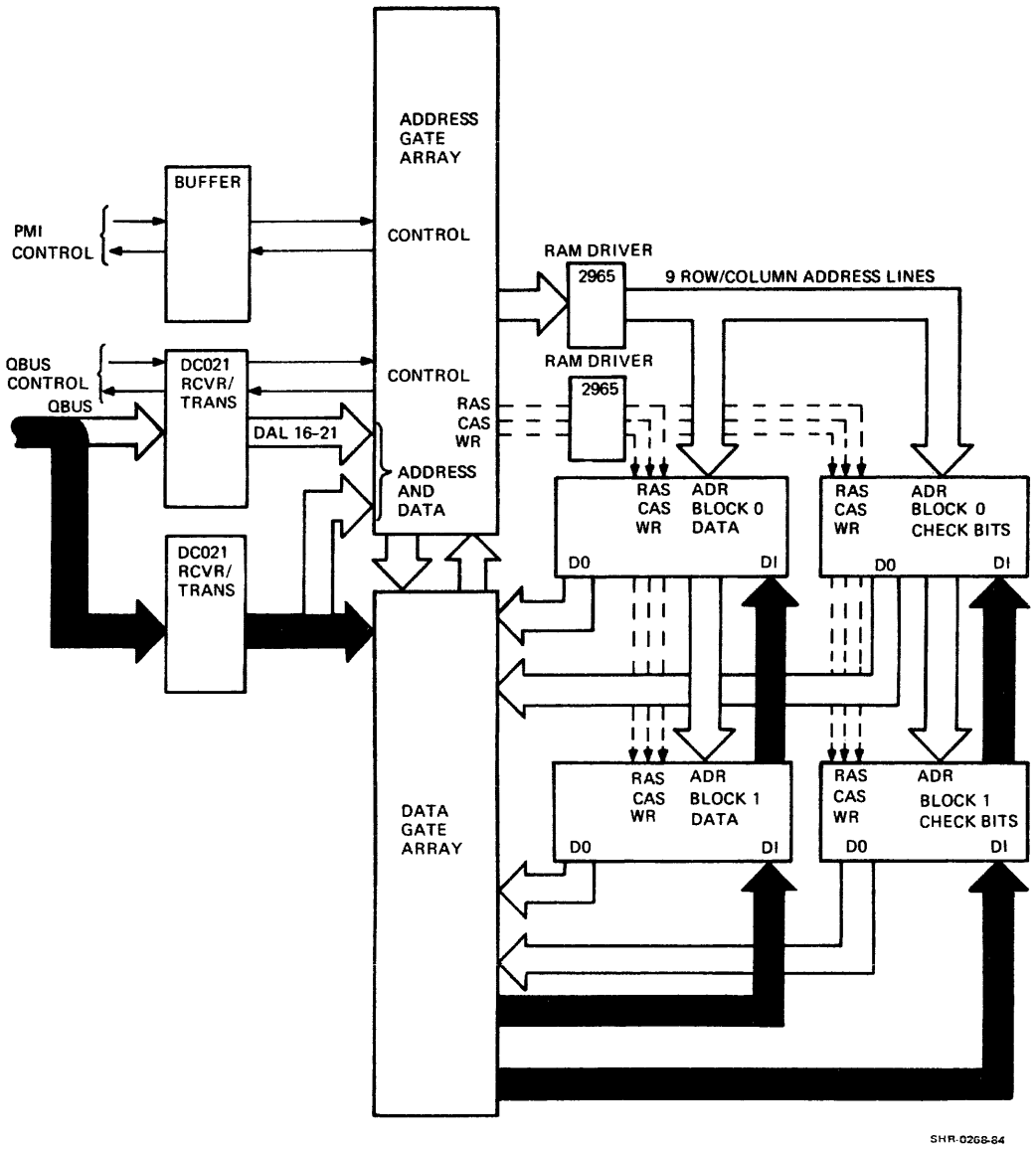


Figure 2-3 Write Cycle Data Flow

2.3.3 Write Byte (Figure 2-4)

The write byte data transfer is actually a read-modify-write to the RAMs. In ECC memory, the check bits are encoded on a 16-bit word basis. Therefore, it is necessary to read the whole word (16 data bits plus 6 check bits) from memory. The word is transferred to the data gate array and checked for errors. If there is a single-bit error, it is corrected.

The processor places a 16-bit word (two bytes) on the Q-bus. One of the two bytes is the byte to be written to memory. This byte is combined in the data gate array with the appropriate byte from memory and a new 16-bit word is formed.

Check bits are calculated on the new 16-bit word resulting in a 22-bit data word. The 22-bit word is then written back to memory.

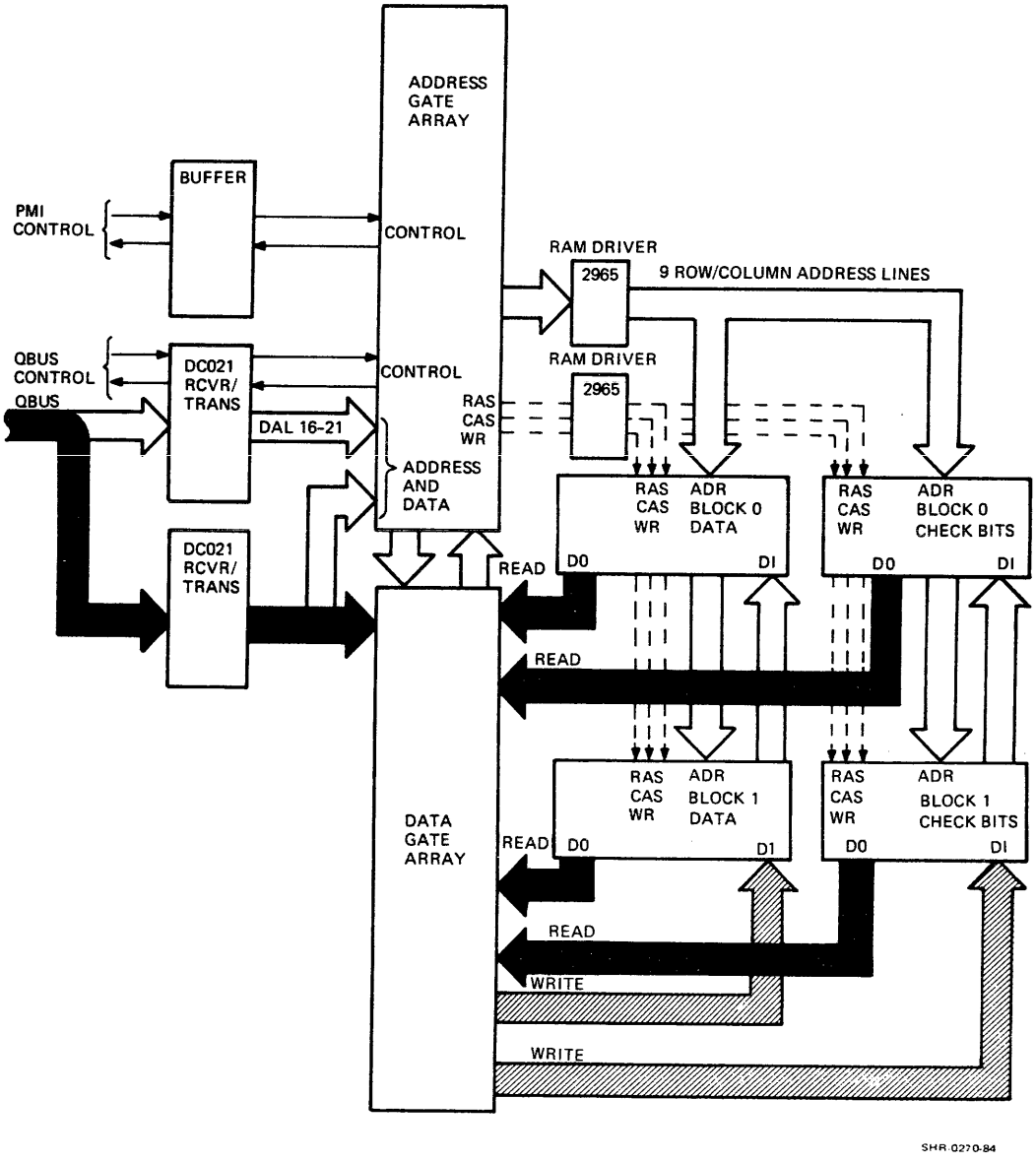


Figure 2-4 Write Byte Cycle Data Flow

Figure 2-5 shows how the write byte operation is performed. The figure assumes the low byte is to be modified. The low byte from the bus is combined in the data gate array with the high byte from memory and a new 16-bit data word is formed. BDAL0 determines the appropriate byte from the bus and the appropriate byte from memory.

If BDAL0=0, the high byte from memory is combined with the low byte from the bus. If BDAL0=1, the low byte from memory is combined with the high byte from the bus.

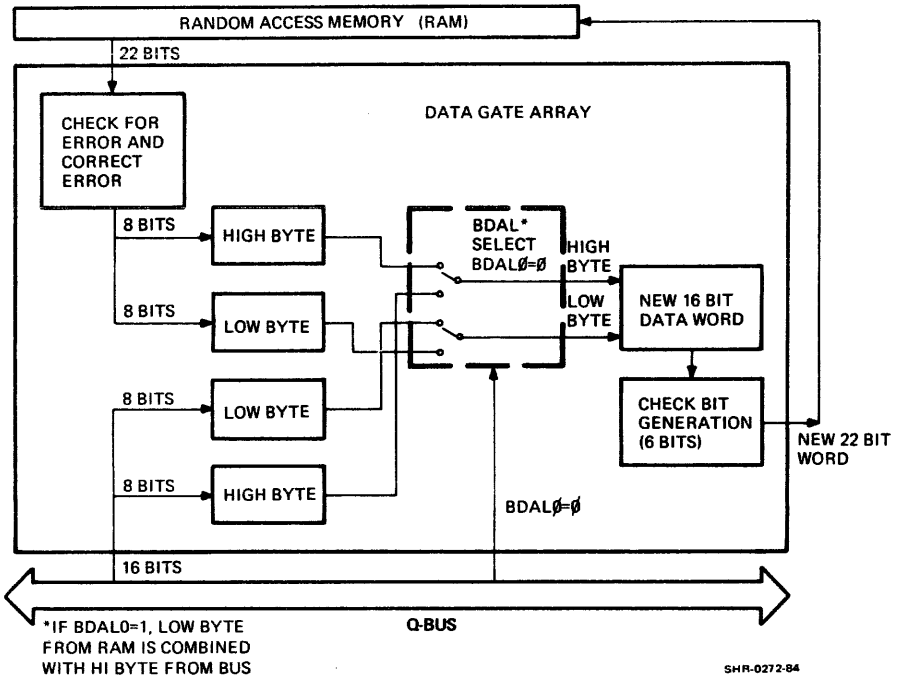


Figure 2-5 Byte Selection for Write Byte Operation

CHAPTER 3
MEMORY CYCLES

3.1 INTRODUCTION

This chapter describes the following types of MSV11-J memory cycles.

- Q-bus (MSV11-JD and MSV11-JE only)
- PMI bus
- Refresh
- ECC initialization (ECC INIT)

Bus cycles are categorized as read, write word, write byte, block mode read, block mode write, read-modify-write, and read-modify-write byte cycles.

Refresh and ECC INIT cycles are internal to the memory. The following paragraphs in this chapter provide additional detail on bus cycles and internal cycles.

3.2 BUS CYCLES

This paragraph describes the basic differences between the Q-bus and PMI bus protocols for the various cycle types.

3.2.1 Read Cycles

Read cycles may be memory read cycles where data is read from RAM, or CSR read cycles where data is read from CSR.

3.2.1.1 Memory Read Cycle – Memory read cycles are two-word reads from RAM. Each word consists of 16 data bits plus 6 check bits.

For Q-bus memory read cycles, two data words are latched into the data gate array. However, only one word is placed on the Q-bus.

For PMI bus memory read cycles, two data words are latched into the data gate array and both words are placed on the bus. Either word may be selected to be placed on the bus first. If the odd word is placed on the bus first, it is followed by the preceding even word. For example, if a word at address 17362 is selected to be placed on the bus first, the next word transferred will be from address 17360. If the even word is selected to be placed on the bus first, the next odd word is then transferred second. For example, if a word at address 17360 is selected to be placed on the bus first, the next word transferred will be at address 17362.

3.2.1.2 CSR Read Cycles – CSR read cycles on the Q-bus and PMI bus are single-word read cycles. No error detection/correction occurs for CSR data.

3.2.2 Write Word Cycles

Write word cycles may be memory write word cycles where data is written in RAM or CSR write word cycles where data is written in the CSR.

3.2.2.1 Memory Write Word Cycles – Memory write word cycles are single-word cycles. After memory receives the data word it generates 6 check bits. The 22 bits are then written to memory.

3.2.2.2 CSR Write Word Cycles – CSR write word cycles on the Q-bus and PMI bus are single write word cycles. Check bits are not generated for CSR write word cycles.

3.2.3 Write Byte Cycle

Q-bus and PMI bus write byte cycles are similar. The check bits for each cycle type are generated by memory on the basis of a 16-bit word. The write byte cycle is executed as a read cycle followed by a write word cycle. The sequence of events is as follows.

1. The word containing the byte to be modified is read from memory and is latched in the data gate array.
2. Error correction occurs if required.
3. The 16-bit data word on the bus containing the new byte is latched in the data gate array.
4. The new byte is combined with the old byte from the memory to form a new 16-bit data word.
5. New check bits are generated for this 16-bit word.
6. The new 22-bit data word is written to RAM.

NOTE: A single-bit error is corrected if one occurs. If a double error occurs, the word cannot be corrected and is written back to memory. No write byte cycle occurs. During subsequent reads of that location, the errors are detected and reported back to the processor.

3.2.4 Block Mode Read Cycles

Q-bus block mode read cycles are successive 16-bit word transfers. Two 16-bit words are read from memory and latched into the data gate array on read cycles. The address gate array takes advantage of this fact during Q-bus block mode read cycles.

During Q-bus block mode transfer, the gate array accesses RAM and a two-word internal read occurs. Both words are latched in the data gate array. Error correction is performed if there is an error. Either one of the two words may be placed on the bus first.

If the processor requests an even word, the even word is placed on the bus. On the next cycle, the odd word, which is already latched in the gate array, is placed on the bus. A second RAM access is not necessary, in this case, as the odd word is already latched in the data gate array (Figure 3-1A).

For example, if the processor requests the data in address 17360, the data in address 17360 and 17362 is latched into the data gate array and the data in address 17360 is placed on the bus. On the next bus cycle, the data in address 17362 (which is latched in the data gate array) is placed on the bus (Figure 3-1A).

If the processor requests an odd word be placed on the bus, that word and the preceding word are latched in the data gate array, and the odd word is placed on the bus. The even word is disregarded as addresses are incremented for block mode read cycles. The next bus cycle causes two more words to be transferred from RAM to the data gate array. The even word is placed on the bus. The odd word is transferred to the bus during the next bus cycle.

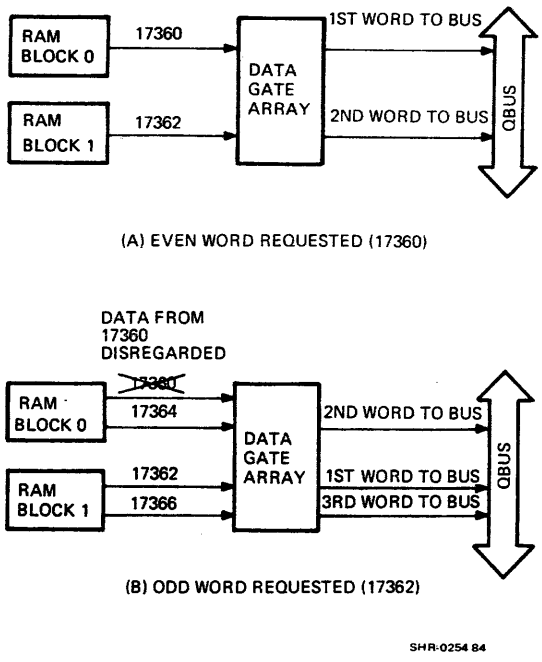


Figure 3-1 Odd/Even Memory Request for Block Mode

For example, if the data in address 17362 is requested to be placed on the bus, the data in address 17360 is disregarded (Figure 3-1B). The next bus cycle causes the data in addresses 17364 and 17366 to be latched in the data gate array. The data in 17364 is placed on the bus. The next cycle causes the data in 17366 to be placed on the bus. Since the data in 17366 was already latched in the data gate array, a RAM access for this data was not required.

PMI bus block mode read cycles always start on even word boundaries and consist of double-word transfers. Two words are placed on the bus during each successive read cycle.

3.2.5 Block Mode Write Cycles

Q-bus block mode write cycles are a succession of single write word cycles to successive memory locations. In the Q-bus write word cycle, there is overhead time between cycles. By using Q-bus block mode write cycles, this overhead is minimized (i.e., no address required in protocol between successive writes).

There are no PMI bus block mode write cycles. In PMI bus write word cycles, the processor can execute the write word cycles very quickly. Therefore, it is not necessary to implement PMI bus block mode write cycles.

3.2.6 Read-Modify-Write Cycle

Memory executes a Q-bus read-modify-write cycle as a read cycle followed by a write cycle to the same location. Memory executes this single-bus cycle as two internal cycles.

There are no read-modify-write cycles in the PMI protocol. A read-modify-write cycle is executed as two bus cycles – a read cycle followed by a separate write cycle to the same location.

3.2.7 Read-Modify-Write Byte Cycle

Memory executes the Q-bus read-modify-write byte as a read cycle followed by a write byte cycle to the same location. Memory executes this single-bus cycle as two internal cycles.

There are no read-modify-write byte cycles in the PMI protocol. A read-modify-write byte cycle is executed as two bus cycles – a read cycle followed by a separate write byte cycle to the same location.

3.3 REFRESH CYCLE

Each memory cell slowly loses its charge so a refresh cycle is needed to restore the contents of memory. Each row of memory must be refreshed every 4 msec.

Refresh is an asynchronous operation whose period is determined by an on-board oscillator. The refresh logic is contained in the address gate array. The array also contains a refresh address counter which keeps track of the rows that are refreshed.

3.4 ECC INIT CYCLE

The ECC INIT cycle is an internal cycle executed only during power up. Its purpose is to write known data into all memory locations soon after power up. Memory writes zeroes in all cells and generates the check bits associated with the cleared memory cells.

A memory location that has not been written to since power up contains unknown random data. If a write byte cycle was performed at that location, an error would most likely occur. In this case, the word read from memory is written back to memory and the write byte cycle aborts. No error indication is flagged. Subsequent read cycles at that same location inform the processor of the error condition.

ECC INIT eliminates the error condition for write byte cycles by clearing the memory cells of invalid data.

For systems without battery backup, ECC INIT occurs when +5 V appears during power up. For systems with battery backup, ECC INIT occurs when the battery backup voltage (+5 VBB) occurs. When +5 V reappears on battery backup systems, ECC INIT is not executed since the data is valid and was not lost.

CHAPTER 4
CONFIGURATION AND CSR OPERATION

4.1 INTRODUCTION

This chapter describes the module installation, control and status register (CSR) operation, operating modes, and error reporting log.

The module installation description includes switch and jumper configurations, memory addressing, CSR addressing, and backplane placements.

The CSR description includes CSR bit format, and descriptions of each bit.

The description of operating modes includes normal modes of operation and various diagnostic modes.

The error reporting description includes error logging performed during PMI bus and Q-bus cycles for single-bit and double-bit errors. From a module viewpoint, errors occurring during read and write byte cycles are latched in the CSR. From the system viewpoint, only uncorrectable errors occurring during read cycles are reported to the central processor. Errors during write byte cycles are not reported.

4.2 MODULE INSTALLATION

Before you remove or replace an MSV11-J memory module, exercise the following cautions.

CAUTION: Static charges can damage the MOS memory chips. Be careful how you handle the module and where you lay it down.

When you install or remove the memory module, make sure there is no dc voltage applied to the module.

If the green LED is on, the module is receiving +5 V from the power supply or battery backup. The power source must be off before you remove or replace a memory module.

4.2.1 Jumper Configurations and Switch Settings

The MSV11-J has jumpers installed at the factory to establish the configuration of the module.

The MSV11-J contains two switchpacks – one is an 8-switch DIP (dual in-line package) and one is a 4-switch DIP. The 8-switch DIP selects the starting memory address on an 8Kword boundary. The 4-switch DIP selects the CSR starting address. One of 16 possible CSR addresses may be selected.

4.2.1.1 Jumper Installation – The following chart summarizes the MSV11-J jumpers (see Figure 4-1).

Jumper	Description
W1 Out	256K dynamic RAMs
W2 In	Half populated module
W2 Out	Fully populated module
W5, W6 mounted horizontally (see Figure 4-2)	Battery backup system
W3, W4 mounted vertically (see Figure 4-3)	+5 V system

NOTE: PDP-11/84 systems are available in a battery backup configuration. In these systems, +5 V BBU is bussed to the +5 V pins in the two slots reserved for the MSV11-J. These memories must NOT be changed to the battery backup configuration.

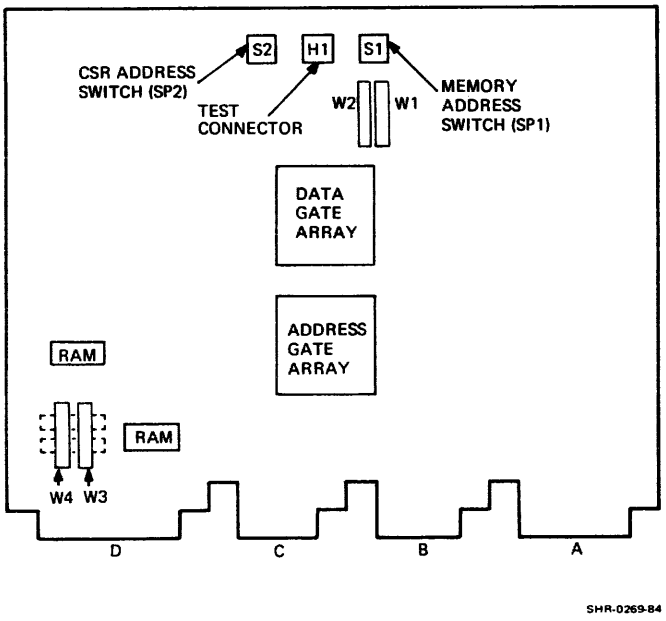


Figure 4-1 MSV11-J Jumpers

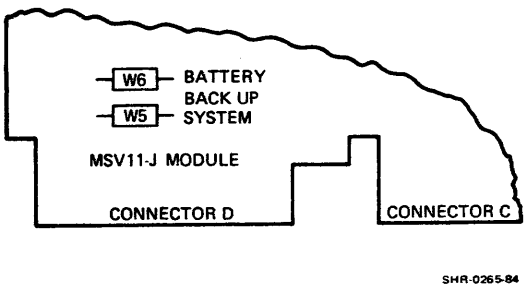


Figure 4-2 Battery Backup Jumper Connection

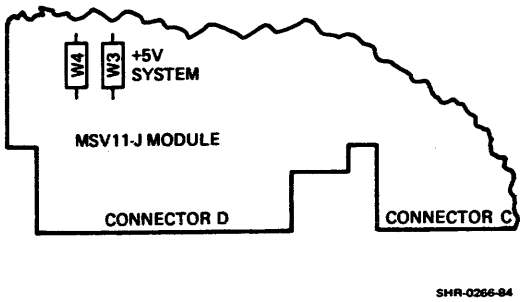


Figure 4-3 +5 V Jumper Connections

4.2.1.2 Memory Address Switch Settings – The memory address switch settings are shown in Table 4-1. The table is divided into 3 columns – the decimal switch settings in 8Kword increments, the octal equivalent, and the actual switch settings shown in binary. The memory address switch (SP1 in Figure 4-1) is an 8-switch DIP (dual in-line package). The least four significant switch settings (5 through 8) of the memory address switch (SP1) represent 8Kword increments as shown in the upper half of the table. For example, if these switch settings (5 through 8) are 0s, a memory address of 0 is represented (assuming switches 1 through 4 are also 0). If switch setting 8 is a 1 (all others being 0s), the memory address is incremented by 8Kwords. If switch setting 7 is a 1, with all other switch settings set to 0, the memory address is incremented by another 8Kwords. The upper half of the table shows the effect of switch settings 5 through 8. Note that switch settings 1 through 4 are all 0s in the upper half of the table and do not come into play until 128Kwords are reached.

The lower half of the table represents increments of 128K until 2 M is reached. Note that switch settings 4 through 1 come into play here. Each increment of these switch settings represents an increase of 128K. For example, if switch setting 4 is a 1 and switch settings 3 through 1 are 0s, a starting address range of 128K to 248K is selected. The specific memory starting address selected within that range is determined by switch settings 8 through 5 (indicated by Xs in the lower half of the table).

Table 4-1 Starting Memory Address Selection

Decimal (Kwords)	Octal	Switch Setting (SP1) 1 2 3 4 5 6 7 8
0	00000000	0 0 0 0 0 0 0 0
8	00040000	0 0 0 0 0 0 0 1
16	00100000	0 0 0 0 0 0 1 0
24	00140000	0 0 0 0 0 0 1 1
32	00200000	0 0 0 0 0 1 0 0
40	00240000	0 0 0 0 0 1 0 1
48	00300000	0 0 0 0 0 1 1 0
56	00340000	0 0 0 0 0 1 1 1
64	00400000	0 0 0 0 1 0 0 0
72	00440000	0 0 0 0 1 0 0 1
80	00500000	0 0 0 0 1 0 1 0
88	00540000	0 0 0 0 1 0 1 1
96	00600000	0 0 0 0 1 1 0 0
104	00640000	0 0 0 0 1 1 0 1
112	00700000	0 0 0 0 1 1 1 0
120	00740000	0 0 0 0 1 1 1 1
000-120	00000000-00740000	0 0 0 0 X X X X
128-248	01000000-01740000	0 0 0 1 X X X X
256-376	02000000-02740000	0 0 1 0 X X X X
384-504	03000000-03740000	0 0 1 1 X X X X
512-632	04000000-04740000	0 1 0 0 X X X X
640-760	05000000-05740000	0 1 0 1 X X X X
768-888	06000000-06740000	0 1 1 0 X X X X
896-1016	07000000-07740000	0 1 1 1 X X X X
1024-1144	10000000-10740000	1 0 0 0 X X X X
1152-1272	11000000-11740000	1 0 0 1 X X X X
1280-1400	12000000-12740000	1 0 1 0 X X X X
1408-1528	13000000-13740000	1 0 1 1 X X X X
1536-1656	14000000-14740000	1 1 0 0 X X X X
1664-1784	15000000-15740000	1 1 0 1 X X X X
1792-1912	16000000-16740000	1 1 1 0 X X X X
1920-2040	17000000-17740000	1 1 1 1 X X X X

NOTE:
1 = Switch on
0 = Switch off
X = Switch can be either on or off

Several examples are provided below to help you understand the table.

Example 1 – Desired starting memory address = 144K

Switch 1234
0001 Selects 128K–248K range
(see lower half of Table 4-1)

```
  144K
 -128K
 ----
   16K
```

5678

0010 represents 16K
(see upper half of Table 4-1)

Starting memory address of 144K = switch settings of:

Switch	12345678
Setting	00010010

Example 2 – Desired starting memory address = 1.576 M

Switch 1234
1100 Selects 1536K to 1656K range
(see lower half of Table 4-1)

```
  1576K
 -1536K
 -----
   40K
```

5678
0101 represents 40K
(see upper half of Table 4-1)

Starting memory address of 1.576 M = switch settings of:

Switch	12345678
Setting	11000101

4.2.1.3 CSR Address Switch Settings – The CSR address switch (Figure 4-1) is a 4-switch DIP (dual in-line package) which allows selection of one of 16 CSR addresses. Table 4-2 shows the possible CSR addresses for 18-bit and 22-bit systems. The switch setting for a particular CSR address is the same whether the CSR is in an 18-bit or 22-bit system. For example, the switch setting is 1110 for a 22-bit CSR address of 17772134 or an 18-bit CSR address of 772134.

Table 4-2 CSR Address Selection

22-Bit CSR Address	18-Bit CSR Address	Switch Setting 1 2 3 4
17772100	772100	0 0 0 0
17772102	772102	0 0 0 1
17772104	772104	0 0 1 0
17772106	772106	0 0 1 1
17772110	772110	0 1 0 0
17772112	772112	0 1 0 1
17772114	772114	0 1 1 0
17772116	772116	0 1 1 1
17772120	772120	1 0 0 0
17772122	772122	1 0 0 1
17772124	772124	1 0 1 0
17772126	772126	1 0 1 1
17772130	772130	1 1 0 0
17772132	772132	1 1 0 1
17772134	772134	1 1 1 0
17772136	772136	1 1 1 1

NOTE:
1 = Switch on
0 = Switch off

4.2.2 Backplane Placements

The PDP-11/83 and PDP-11/84 system backplanes are designed for the MSV11-J memory which incorporate Q-bus and PMI-bus protocols. The MSV11-JB and MSV11-JC memory variations can only be used in PDP-11/84 systems. The MSV11-JD and MSV11-JE variations can be used in PDP-11/84 or PDP-11/83 systems.

As a cross-product, the MSV11-J memory can be installed in a Q-CD backplane. However, you must not install an option in a slot adjacent to the MSV11-J that uses pins in the CD connector. Instead, leave an empty slot between the MSV11-J and this option. An option which does not use pins in the CD connector may be placed adjacent to the MSV11-J.

NOTE: Do not install the MSV11-J in a Q-Q backplane since this backplane shorts Q-bus signals to PMI bus signals and the system will not operate. This can also result in damage to the MSV11-J and other modules in a Q-Q backplane.

The location of the MSV11-J memories in a PDP-11/83 system determine the protocol to be used between memory and CPU. For PMI protocol, the MSV11-Js must be located immediately in front (lower slot number) of the CPU; otherwise the memory and CPU will communicate with the Q-bus protocol.

Table 4-3 shows the backplane pin assignments. Connectors A through D are shown across the top and pin numbers A through V (excluding G, I, O, and Q) are listed down the side. Backplane pins are designated first by slot, then by pin number, and then by the side of the module. A typical example is shown below.

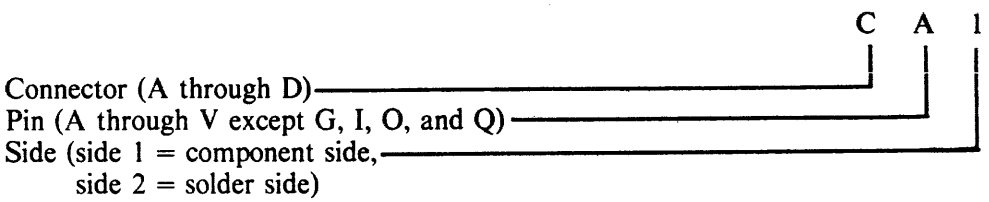


Table 4-3 Backplane Pin Utilization

Pin	Connector A Side 1	Connector A Side 2	Connector B Side 1	Connector B Side 2	Connector C Side 1	Connector C Side 2	Connector D Side 1	Connector D Side 2
A		5V	BDCOK	5V	S RUN	5V	PBYT	5V
B			BPOK		PSSEL	PSSEL	PWTSTB	PWTSTB
C	BDAL16	GND	BDAL18	GND	S RUN	GND	PBYT	GND
D	BDAL17		BDAL19		PUBMEM	PUBMEM	PMAPE	PMAPE
E		BDOUT	BDAL20	BDAL2	PBCYC	PBCYC		
F		BRPLY	BDAL21	BDAL3	PUBSYS	PUBSYS		
H		BDIN		BDAL4	PHBPAR	PHBPAR		
J	GND	BSYNC	GND	BDAL5	PSBFUL	PSBFUL		
K	REF KILL	BWTBT		BDAL6	PLBPAR	PLBPAR		
L				BDAL7				
M	GND	BIAKI	GND	BDAL8	PRDSTB	PRDSTB		
N		BIAKO		BDAL9				
P		BBS7		BDAL10	PBLKM	PBLKM		
R	BREF	BDMGI		BDAL11	PBSY	PBSY		
S		BDMG0		BDAL12			BBSY	BBSY
T	GND	BINIT	GND	BDAL13	GND		GND	
U		BDAL0		BDAL14			5VBBU	5VBBU
V	5VBBU	BDAL1	5V	BDAL15	PUBTMO	PUBTMO	5VBBU	5VBBU

NOTES:
1. *CA1 is connected to CC1 on the module*
2. *DA1 is connected to DC1 on the module*
3. *All PMI signals except PBYT have the connectors on side 1 etched to the respective signal on side 2 of the module*
4. *AM2 is connected to AN2 on the module*
5. *AR2 is connected to AS2 on the module*
6. *Side 1 is component side*
7. *Side 2 is back side*

4.3 CONTROL AND STATUS REGISTER (CSR)

The control and status register in the MSV11-J allows program control of certain ECC functions and contains diagnostic information if an error has occurred. The CSR is a 16-bit register and has an assigned address – it can be accessed via the Q-bus, or PMI protocol.

There is one CSR per memory module. Each CSR can be assigned to one of 16 predetermined addresses which range from 772100 to 772136 for 18-bit systems and from 17772100 to 17772136 for 22-bit systems (refer to Table 4-2).

ECC is performed only on memory accesses and is not used when accessing the CSR.

4.3.1 Bit Format of CSR

Figure 4-4 shows the bit assignments of the CSR. Unused bits are read as 0.

4.3.2 Bit Descriptions of CSR

Table 4-4 describes each of the CSR bits shown in Figure 4-4.

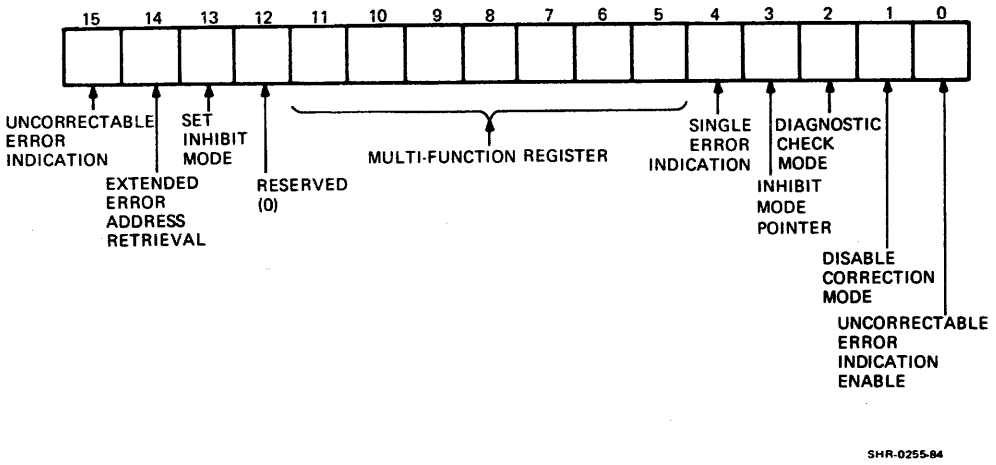


Figure 4-4 CSR Bit Assignments

Table 4-4 CSR Bit Descriptions

Bit	Name	Set By Cleared By	Remarks
00	Uncorrectable error indication enable read/write	Set/cleared by software Cleared by power up and BUS INIT	Does not affect CSR. BDAL17 is driven directly by CSR00 at same time as data during a DATI(O) cycle. BDAL16 is not affected by CSR00. CSR00=0 Inhibit Error Indication Will not allow a system parity (uncorrectable error) trap; i.e., BDAL17 is not asserted with data on DATI(O) cycles during uncorrectable error detection. CSR04 and CSR15 still indicates errors. BDAL16 is asserted with data on DATI(O) cycle when an uncorrectable error occurs. CSR00=1 Active Error Indication This bit causes assertion of BDAL17 with data during all DATI(O) cycles.

Table 4-4 CSR Bit Descriptions (Cont)

Bit	Name	Set By Cleared By	Remarks
01	Disable correction mode read/write	Set/cleared by software Cleared by power up and BUS INIT	Serves as a diagnostic aid to allow reading data from memory without interference from the error correction logic. CSR01=0 Enable Error Correction Single error sets CSR04 and latches error address and syndrome bits. Double error sets CSR15 and latches error address and syndrome bits. Once a double error is detected, a single error is flagged through CSR04, but does not cause the address and syndrome bits to be overwritten. CSR01=1 Disable Error Correction Single error is uncorrectable, and sets CSR04 and CSR15. Double error sets CSR15 only. Priority of single and double error address and syndrome bit latch are the same.
02	Diagnostic check mode read/write	Set/cleared by software Cleared by power up and BUS INIT	This mode allows the forcing of a single or double error in a desired location. Also provides a means of examining the check bits and syndrome bits in a given location. The check bits for a given 16 bit data pattern are written into bits 5 through 10 of the CSR. Subsequent DATO or DATOB cycles write the check bits from the CSR to the MOS array in diagnostic mode (CSR2 set). During DATI or DATIO cycles check bits from memory are latched into the CSR. In the diagnostic mode, CSR04 and CSR15 react to single and double errors; address and syndrome bits are not logged. Single-bit errors are corrected on DATI and DATOB cycles. CSR2=0 Normal Operation CSR2=1 Diagnostic Mode Next DATI stores RAM array check bits into CSR05 through CSR10. Next DATO writes CSR05 through CSR10 into RAM array check bits.

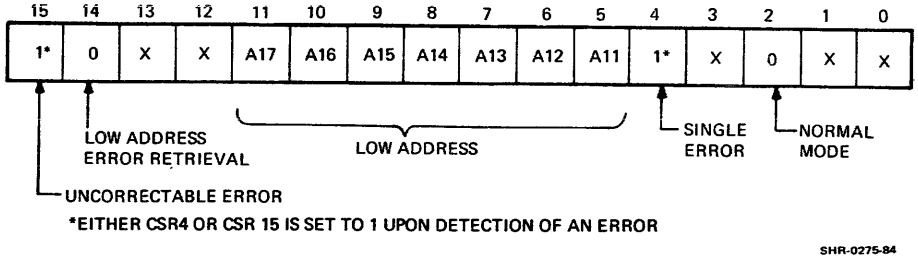
Table 4-4 CSR Bit Descriptions (Cont)

Bit	Name	Set By Cleared By	Remarks
03	Inhibit mode pointer read/write	Set/cleared by software Cleared by power up and BUS INIT	This bit works in conjunction with set inhibit mode (CSR13). If CSR13=1 and CSR03=0, the first block (0 to 16Kwords) of memory cannot operate in ECC disable mode or diagnostic check mode. If CSR13=1 and CSR03=1, the second block (16Kwords to 32Kwords) of memory cannot operate in these modes. Therefore CSR03, in conjunction with CSR13, allows a 16K block of memory to always have ECC coverage (protected). The system diagnostic can therefore reside in this protected portion of memory and can disable ECC and/or run the Diagnostic Check Mode in the rest of memory without itself becoming vulnerable to single errors. *NOTE: A memory resident diagnostic must always be protected. If not protected from the diagnostic check mode or the disable correction mode, a memory resident diagnostic produces errors.* If CSR13=0 CSR03 is inoperative If CSR13=1 CSR03 is operative CSR03=0 0–16 kW ECC protect CSR03=1 16 kW–32 kW ECC protect
04	Single error read/write	Set by a single bit error Set/cleared by software Cleared by power up and BUS INIT	Set upon detection of a single error if: CSR01=0 or CSR01=1, AND CSR13=1 AND CSR03 is protecting an accessed word. CSR4=0 No single errors detected CSR4=1 Single error detected
05 – 11	Multifunction register bits read/write	Set by software NOT cleared by power up or BUS INIT	These seven bits log check bits in diagnostic mode or log multiplexed address and syndrome bits in normal mode.

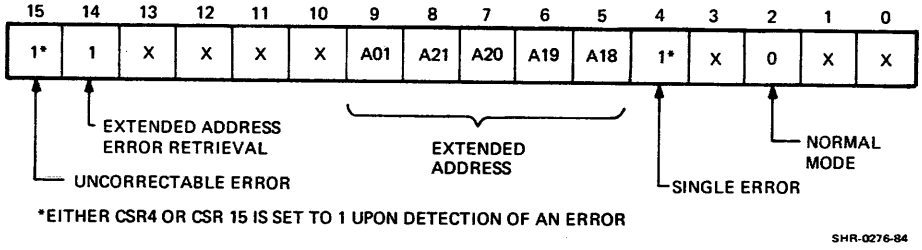
Table 4-4 CSR Bit Descriptions (Cont)

Logging of Address, Syndrome, and Check Bits

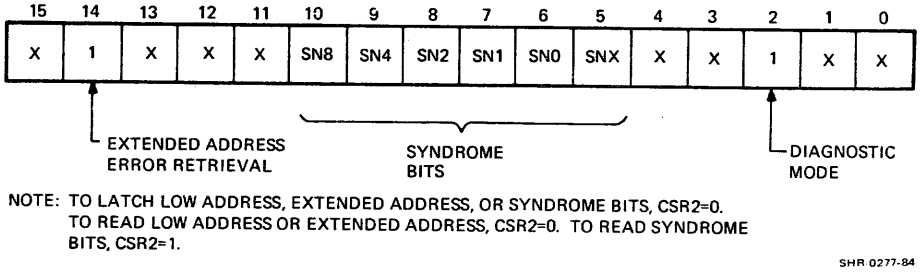
After a failure, the address and syndrome bits are logged in the CSR. The address is recovered in normal mode (CSR2=0) and the syndrome bits are recovered in diagnostic mode (CSR2=1) as described below.



To recover address bits 11 through 17 (low address retrieval), CSR2 is set to 0, CSR14 is set to 0, either CSR4 or CSR15 is set to 1, and CSR5 through CSR11 contain A11 through A17 of the failed memory address.



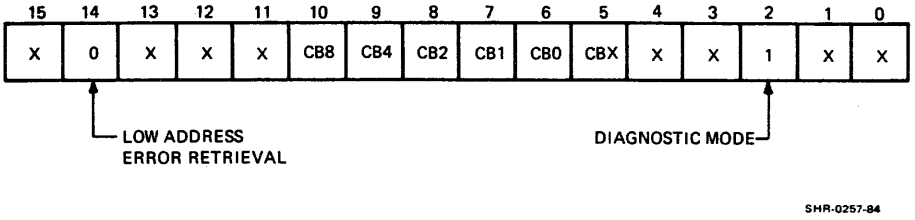
To recover address bits A18 through A21 and A01 (extended address retrieval), CSR2 is set to 0, CSR14 is set to a 1, and CSR bits 5 through 9 contain A18 through A21 and A1 of the failed memory address.



During normal operation (CSR2=0), a single- or double-bit error causes the address and syndrome bits to be latched in the CSR. To recover the syndrome bits, CSR2 is set (diagnostic mode) and CSR14 is set. During a CSR read, CSR05 through CSR10 contain the previously latched syndrome bits (SnX, Sn0, Sn1, Sn2, Sn4, Sn8).

Table 4-4 CSR Bit Descriptions (Cont)

Logging of Address, Syndrome, and Check Bits



During DATI cycles, check bits from memory are written into CSR5 through CSR10 regardless of any errors at that memory location.

During DATO(B) cycles, contents of CSR5 through CSR10 are written into check bits of that memory location regardless of any errors at that location.

To recover the check bits, CSR2 is set (diagnostic mode) and CSR14 is cleared. CSR5 through CSR10 will contain the memory locations check bits after a DATI cycle. If a DATO(B) cycle is executed, CSR5 through CSR10 contain the check bits to be written to memory.

Bit	Name	Set By Cleared By	Remarks
12	Reserved		Always read as 0
13	Set inhibit mode read/write	Set/cleared by software Cleared by power up and BUS INIT	When this bit is cleared in diagnostic mode (CSR2=1), it allows the diagnostic check mode and/or ECC disable mode to operate throughout the MSV11-J memory. When this bit is set, it enables the inhibit mode pointer to inhibit either the first 16Kwords or second 16Kwords segment from entering diagnostic mode or ECC disable mode. CSR3 determines which 16Kwords is protected from entering diagnostic mode (CSR2=1) or ECC disable mode (CSR1=1). CSR 13=0 enable diagnostic check mode and ECC disable mode CSR13=1 inhibit diagnostic check mode and ECC disable mode

Table 4-4 CSR Bit Descriptions (Cont)

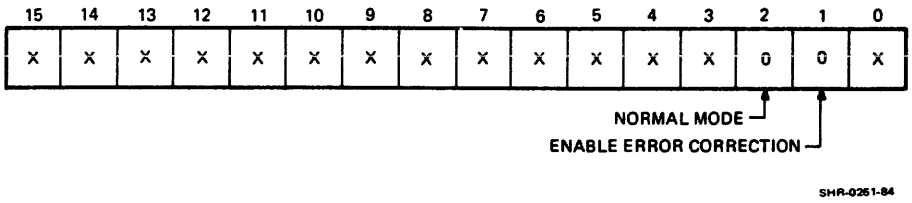
Bit	Name	Set By Cleared By	Remarks
14	Extended error address retrieval read/write	Set/cleared by software Cleared by power up and BUS INIT	CSR 14=0 Retrieve Low Address (A11 - A17) CSR 14=1 Retrieve High Address (A18 - A21 and A01) Multiplexes low address (A11 through A17) and extended address (A18 through A21 and A01) to CSR05 through CSR11 in normal mode (CSR2=0). If CSR14 is reset, a CSR read presents A11 through A17 to CSR05 through CSR11. If CSR14 is set, a CSR read presents A18 through A21 and A01 to CSR5 through CSR9. *NOTE: With CSR14 on a 1, diagnostic data may not be loaded into the CSR syndrome register.*
15	Uncorrectable error read/write	Set by uncorrectable error Set/cleared by software Cleared by power up and BUS INIT	Set if an uncorrectable error is detected; i.e., two or more errors with ECC enabled (CSR1=0) or one or more errors with ECC disabled (CSR1=1). CSR15=0 No uncorrectable error detected CSR15=1 Uncorrectable error detected CSR1=0 Two or more errors CSR1=1 One or more errors

4.3.3 Operating Modes

The MSV11-J uses seven operating modes to control error logging and error reporting during memory bus cycles.

These modes are shown in Table 4-5. The CSR bit settings for the seven modes are also shown. For example, in normal mode, CSR1 is cleared (error correction enabled) and CSR2 is cleared (normal mode).

4.3.3.1 Normal Mode (ECC Enabled)



The memory usually operates in normal mode. Single- and double-bit error status is recorded in CSR 04 and CSR 15, respectively. Error address and syndrome bits are stored in multifunction register bits CSR 5 through CSR 11. This paragraph describes the error conditions for the various cycle types in this mode. They are listed below.

Read Cycle – Single Error

- CSR 4 – single error is set.
- CSR 15 (uncorrectable error indication) is unaffected.
- Data is corrected by error detection logic before being placed on the bus.
- If CSR 15 has not previously been set, A11 through A21, A01, and the error syndrome bits are latched in the CSR.
  If CSR 15 has been set, the address and syndrome bits are unaffected. (Single-bit error status does not override previously latched double-error status.)

Read Cycle – Double Error

- CSR 4 is unaffected.
- CSR 15 is set.
- Red LED is on.
- A11 through A21, A01, and the error syndrome bits are latched in the CSR. (Double-bit errors override single-bit errors.)
- Error asserts BDAL 16L (uncorrectable error) during the data portion of the read cycle.

Write Byte Cycle – Single Error During Read Portion

- CSR 4 is set.
- CSR 15 is unaffected.
- If CSR 15 has not previously been set, A11 through A21, A01 and the error syndrome bits are latched in the CSR. If CSR bit 15 is set, the address and syndrome bits are unaffected.
- The error in the data is corrected and is combined with the new byte.
- Check bits are generated on the new 16-bit data word.
- The new data word and new check bits are written to memory.

Write Byte Cycle – Double Error During Read Portion

- CSR 15 is not set.
- Address and syndrome bits are NOT logged.
- Error is preserved by writing the old data and check bits back to memory. The new byte is lost.
- Error will be detected on the next DATI cycle to that location.

Write Word Cycle

- CSR 4 and CSR 15 are unaffected.
- Check bits generated by ECC.
- Data and check bits are written into memory.

Address and Syndrome Retrieval

1. Read CSR
   If CSR 14=0, then CSR 5 through 11 contains A11 through A17 of the failed address.
   If CSR 14=1, then CSR 05 through 9 contains A18 through A21 and A01 of the failed address.

2. Write CSR
   Change the state of CSR 14 to obtain the other half of the stored address.
   If CSR 14 was 0, then change to 1.
   If CSR 14 was 1, then change to 0.

3. Read CSR
   CSR 05 through CSR 11 (or CSR 05 through CSR 09) contain the other half of the address (see step 1).

4. Write CSR to diagnostic mode
   Set CSR 02=1, CSR 14=1

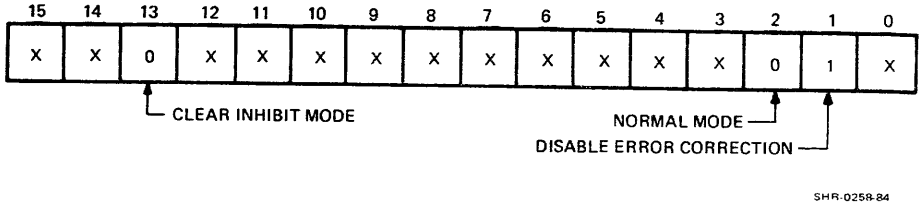
5. Read CSR (diagnostic mode)
   CSR 5 through CSR 10 contains the six syndrome bits.

Table 4-5 Operating Modes

Mode	CSR Bit Settings 15	14	13 4	3	2	1	0
Normal, ECC enabled	X	X	0	X	X	0	0	X
Normal, ECC disabled	X	X	0	X	X	0	1	X
Normal mode, ECC disabled, protected*	X	X	1	X	0,1	0	1	X
Diagnostic mode, ECC enabled	X	X	0	X	X	1	0	X
Diagnostic mode, ECC disabled	X	X	0	X	X	1	1	X
Diagnostic mode, ECC enabled, protected*	X	X	1	X	0,1	1	0	X
Diagnostic mode, ECC disabled, protected*	X	X	1	X	0,1	1	1	X

* Protected mode refers to the first 16Kwords or second 16Kwords of memory which is protected from entering diagnostic mode or ECC disable mode. The 16Kword area selected is accomplished via CSR bit 3. If this bit is 0, the first 16Kwords are protected and if the bit is a 1, the second 16Kwords are protected.

4.3.3.2 Normal Mode (ECC Disabled)



Normal mode with ECC disabled inhibits the correction of a single-bit error. Generation of check bits is not inhibited by this mode. All detected errors are considered uncorrectable.

This mode is used to gain visibility of normally corrected single bit memory errors. The error conditions for the various cycle types are listed below.

Read Cycle - Single Error
- CSR 15 AND CSR 4 are set. Single error is uncorrectable.
- Red LED is on.
- All through A21, A01, and syndrome bits are latched in the CSR.
- BDAL 16 is asserted on the bus during the data portion of the read cycle.

Read Cycle - Double Error
- CSR 15 is set, CSR 4 is unaffected.
- Red LED is on.
- All through A21, A01 and error syndrome bits are latched in CSR.
- Error asserts BDAL 16 during the data portion of the read cycle.

Write Byte Cycle - Single Error During Read Portion
- CSR 15 AND CSR 4 are set. Single error is corrected.
- Red LED is on.
- Address and syndromes are latched in the CSR.
- Data containing error is corrected, then combined with new byte.
- Check bits are generated by the ECC on the new word.
- New word and check bits are written into memory.

Write Byte Cycle - Double Error During Read
- CSR 15 is NOT set
- Address and syndromes are NOT latched in the CSR.
- Error is preserved by writing the old data and check bits back into memory. The new byte is lost. Error is detected on the next DATI cycle to that location.

Write Word Cycle
- Check bits are generated by ECC on the new word.
- Data and check bits are written into memory.

Address and Syndrome Retrieval
1. Read CSR
   If CSR 14=0, then CSR 05 through 11 contains A11 through A17 of the failed address.
   If CSR 14=1, then CSR 05 through 09 contains A18 through A21 and A01 of the failed address.

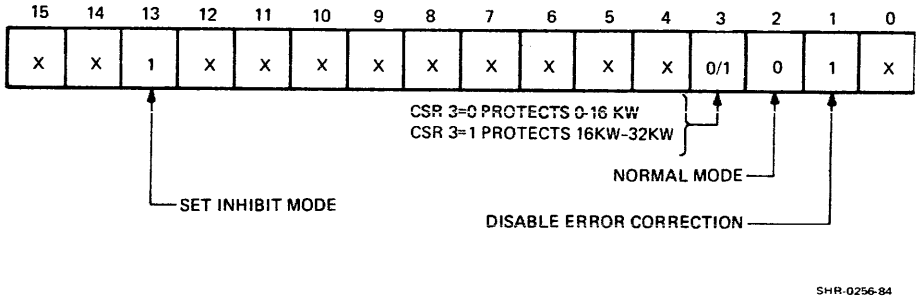
2. Write CSR, Change CSR 14
   If CSR 14 was 0, then change to 1.
   If CSR 14 was 1, then change to 0.

3. Read CSR
   CSR 05 through 11 (CSR 05 through 09) contain the other half of the address (see step 1).

4. Write CSR (Enter Diagnostic Mode)
   Set CSR 02=1, CSR 14=1.

5. Read CSR
   CSR 05 through 10 contains syndrome bits.

4.3.3.3 Normal Protected Mode (ECC Disabled)



One of two 16 kW blocks may be protected from the ECC disable mode (CSR 01=1, CSR 13=1, CSR 03=0 to protect first 16K and CSR 01=1, CSR 13=1 and CSR 3=1 to protect second 16K of memory). Single-bit errors are corrected as in the normal mode with ECC enabled. This feature provides protection for the memory resident diagnostic.

The error conditions for the various cycle types in this mode are listed below.

Read Cycle - Single Error
- CSR 4 and CSR 15 are NOT set.
- Data is corrected by the ECC before being put on the bus.
- Address and syndromes are NOT latched in the CSR.

Read Cycle - Double Error
- CSR 15 is set.
- Red LED is on.
- Address and syndromes are latched in the CSR.
- Error causes BDAL 16 to be asserted at the same time as (uncorrected) data.

Write Byte Cycle - Single Error During Read Portion
- CSR 4 is NOT set.
- Address and syndromes are NOT latched in CSR.
- Old data is corrected and combined with new byte.
- Check bits are generated by ECC on the new word.

Write Byte Cycle - Double Error During Read Portion
- CSR 15 is NOT set.
- Address and syndromes are NOT latched in CSR.
- Write byte is not executed, old data and check bits are written back into memory, preserving error in that location.
- New data is lost.

Write Word Cycle
- Check bits are generated by the ECC on the new memory.
- Data and check bits are written into memory.

Address and Syndrome Retrieval
1. Read CSR
   If CSR 14=0, then CSR 05 through 11 contains A11 through A17 of the failed address.
   If CSR 14=1, then CSR 05 through 09 contains A18 through A21 and A01 of the failed address.

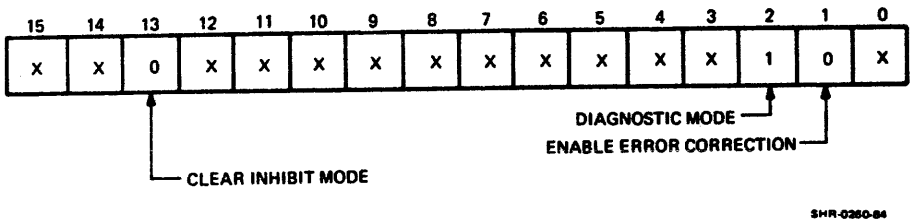
2. Write CSR change CSR 14.
   If CSR 14 was 0, then change to 1.
   If CSR 14 was 1, then change to 0.

3. Read CSR
   CSR 05 through 11 (or CSR 05 through 09) contains the other half of the address (see step 1).

4. Write CSR (Enter Diagnostic Mode)
   Set CSR 02=1, CSR 14=1

5. Read CSR
   CSR 05 through 10 contains syndrome bits.

4.3.3.4 Diagnostic Mode (ECC Enabled)



Diagnostic mode allows the ECC of the MSV11-J to be tested. An error may be simulated by writing 'wrong' check bit data into a memory location. This error should be detected and corrected on a subsequent read from that location. Data written into CSR 05 through CSR 11 in the diagnostic mode is substituted for the generated check bits (from the parity tree logic) on subsequent DATO cycles.

Incorrect check bits can be written to any memory location in this manner. Subsequent DATI cycles to any of these locations (while in normal mode) cause error logging.

Additionally, the check bits from a memory location are latched into CSR 05 through CSR 11 during a DATI cycle. The bus master can force check bits during DATO cycles, it can read check bits during DATI cycles.

The error conditions for the various cycle types in this mode are listed below.

Read Cycle - No Errors
- Data is read from memory and placed on the bus.
- Check bits read from memory are latched in CSR 5 through CSR 10.

Read Cycle - Single Error
- CSR 4 is set.
- Data is read from memory and corrected before being placed on the bus.
- Check bits read from memory are always latched in CSR 5 through CSR 10.
- Address and error syndrome bits are NOT latched in the CSR.

Read Cycle - Double Error
- CSR 15 is set
- Red LED is on.
- Check bits read from memory are latched in CSR 5 through CSR 10.
- Address and error syndrome bits are NOT latched in the CSR.
- Error asserts BDAL 16 during the data portion of the read cycle.

Write Byte Cycle - No Errors
- New byte is combined with old byte and written to memory.
- Check bits from CSR 5 through CSR 10 (instead of the ECC) are written into memory.

Write Byte Cycle – Single Error During Read Portion

- CSR 4 is NOT set.
- Data containing error is corrected and combined with the new byte.
- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.
- Address and syndromes are NOT latched in the CSR.

Write Byte Cycle – Double Error During Read Portion

- CSR 15 is NOT set.
- Address and syndromes are NOT latched in the CSR.
- Error is ignored.
- New byte is combined with the old byte.
- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.

Write Word Cycle

- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.

Check Bit Retrieval

1. Must be in diagnostic mode (CSR 2=1, CSR 14=0)
   Read memory location
   Check bits from RAMs are latched in CSR 5 through CSR 10.

2. Read CSR
   CSR 5 through CSR 10 contain check bits Cbx, Cb0, Cb1, Cb2, Cb4, and Cb8.

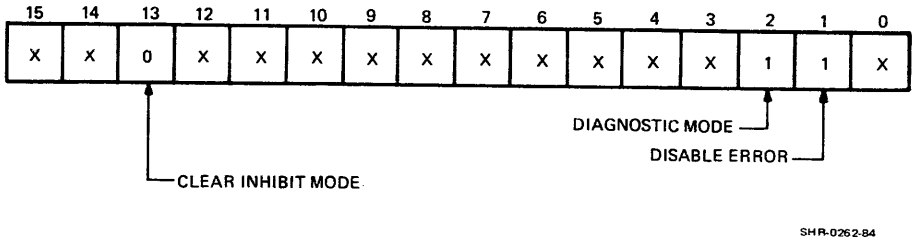
Inserting Check Bits (for checking ECC logic)

1. Write check bit pattern into CSR 5 through CSR 10 (CSR 2=1).

NOTE: If the memory is in the normal mode, this step takes two writes to the CSR. The first CSR write puts the memory in the diagnostic mode, the second write loads check bit data in CSR 5 through CSR 10.

2. Write to a memory location.
   The contents of CSR 5 through CSR 10 are written to that locations check bit RAMs (Cbx, Cb0, Cb1, Cb2, Cb4 and Cb8).

4.3.3.5 Diagnostic Mode (ECC Disabled)



This mode is a variation of the diagnostic mode. Check bits can be written and read through the CSR as described in the Diagnostic Mode. Single-bit errors are not correctable in this mode so they are reported as uncorrectable.

The error conditions for the various cycle types in this mode are listed below.

Read Cycle - No Errors
- Data is read from memory and placed on the bus.
- Check bits read from memory are latched in CSR 5 through CSR 10.

Read Cycle - Single Error
- CSR 4 and CSR 15 are set. Single error is uncorrectable.
- Red LED is on.
- DATA is NOT corrected. Uncorrected data is placed on the bus.
- Check bits read from memory are always latched in CSR 5 through CSR 10.
- Address and error syndrome bits are not latched in the CSR.
- BDAL 16 is asserted on the bus during the data portion of the read cycle.

Read Cycle - Double Error
- CSR 15 is set.
- Red LED is on.
- Check bits read from memory are latched in CSR 5 through CSR 10.
- Address and error syndrome bits are NOT latched in the CSR.
- Error asserts BDAL 16 during the data portion of the read cycle.

Write Byte Cycle - No Errors
- New byte is combined with old byte and written to memory.
- Check bits come from CSR 5 through CSR 10 (instead of the ECC) and are written into memory.

Write Byte Cycle - Single Error During Read Portion
- CSR 4 is NOT set.
- Data containing error is corrected and combined with the new byte.
- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.
- Address and syndromes are NOT latched in the CSR.

Write Byte Cycle - Double Error During Read Portion
- CSR 15 is NOT set.
- Address and syndromes are NOT latched in the CSR.
- Error is ignored.
- New byte is combined with the old byte.
- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.

Write Word Cycle
- Check bits come from CSR 5 through CSR 10.
- Data and check bits are written into memory.

Check Bit Retrieval
1. Must be in the diagnostic mode (CSR 2=1, CSR 14=0).
   Read memory location.
   Check bits from RAMs are latched in the CSR (CSR 5 through CSR 10).
2. Read CSR
   CSR 5 through CSR 10 contain check bits (Cbx, Cb0, Cb1, Cb2, Cb4, and Cb8).

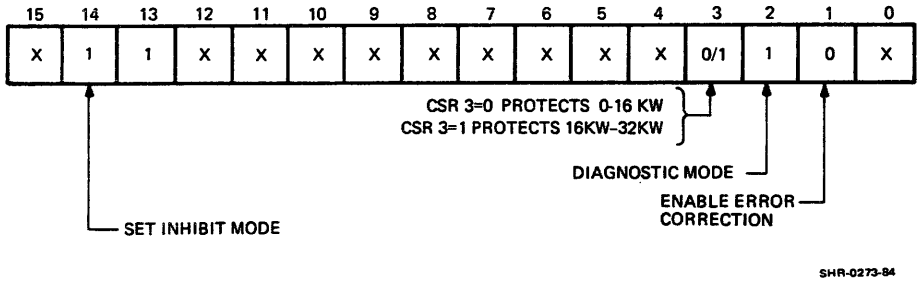
Inserting Check Bits

1. Write check bit pattern into CSR 5 through CSR 10 (CSR 2=1).

NOTE: If the memory is in normal mode, this step takes two writes to the CSR. The first CSR write puts the memory in the diagnostic mode, the second write loads check bit data in CSR 5 through CSR 10.

2. Write to a memory location.
   The contents of CSR 5 through CSR 10 are written to that location's check bit RAMs (Cbx, Cb0, Cb1, Cb2, Cb4, and Cb8).

4.3.3.6 Protected Diagnostic Mode (ECC Enabled)



Protected diagnostic mode may be enabled while in diagnostic mode. This protected mode protects one of two 16 kW blocks of memory where the diagnostic program resides. The protected block remains protected by the error correction logic.

The error conditions for the various cycle types in this mode are listed below.

Read Cycle - No Errors

- Data is read from memory as in the normal operating mode.
- Check bits read from memory are NOT latched in CSR 5 through CSR 10.

Read Cycle - Single Error

- CSR 4 is set.
- Check bits are NOT latched in CSR 5 through CSR 10.
- Data is corrected by the ECC before being put on bus.
- Address and syndromes are NOT latched in the CSR.

Read Cycle - Double Error

- CSR 15 is set.
- Red LED is on.
- Check bits read from memory are NOT latched in CSR 5 through CSR 10.
- Address and error syndrome bits are NOT latched in the CSR.
- Error asserts BDAL 16 during the data portion of the read cycle.

Write Byte Cycle - Single Error During Read Portion

- CSR 4 is set.
- Address and syndromes are NOT latched in CSR 5 through CSR 10.
- Data containing error is corrected and combined with new byte.
- Check bits are generated by ECC on the new word.

Write Byte Cycle – Double Error During Read Portion

- CSR 15 is NOT set.
- Address and syndromes are NOT latched.
- Error is preserved by writing the old data and check bits back into memory. The new byte is lost. Error is detected on the next DATI cycle to that location.

Write Word Cycle

- Check bits are generated by the ECC.
- Check bits and data are written into memory.

Address, Syndrome, Check Bit Retrieval

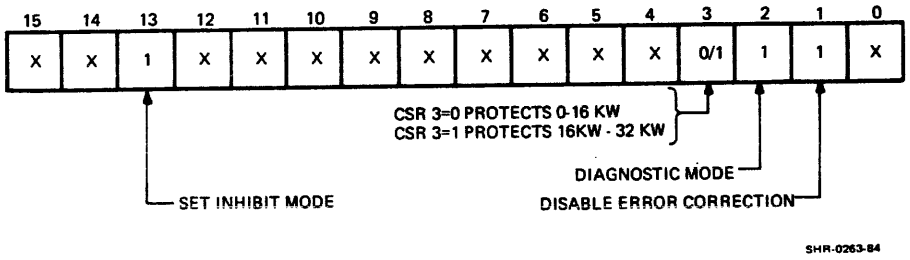
The diagnostic protected 16 kW block of memory stores the memory resident diagnostic. CSR 3 selects the 16 kW block to be protected. This block, therefore, behaves as though it were in the normal mode with ECC enabled. Check bits are not latched.

Address and syndrome bits are not latched while in this mode. The CSR is intended for check bit storage for the memory under test (not protected).

Inserting Check Bits

Check bits are not written from the CSR to the RAM check bits while in the protected block. This protected block behaves as though it were in normal mode with ECC enabled. Check bits are generated by ECC.

4.3.3.7 Protected Diagnostic Mode (ECC Disabled)



This mode (a variation of the protected diagnostic mode) protects one of two 16 kW blocks of memory where the diagnostic program resides. This block of memory remains protected by the error correction logic and therefore behaves as though it were in the normal mode with ECC enabled. Check bits are not latched and single-bit errors are corrected.

The error conditions for the various cycle types in these modes are listed below.

Read Cycle – No Errors
- Data is read from memory as in the normal operating mode.
- Check bits read from memory are NOT latched in CSR 5 through CSR 10.

Read Cycle – Single Error
- CSR 4 is set.
- Check bits are NOT latched in CSR 5 through CSR 10.
- Data is corrected by the ECC before being put on bus.
- Address and syndromes are NOT logged in the CSR.

Read Cycle – Double Error
- CSR 15 is set.
- Red LED is on.
- Check bits read from memory are NOT latched in CSR 5 through CSR 10.
- Address and error syndrome bits are NOT latched in the CSR.
- Error asserts BDAL 16 during the data portion of the read cycle.

Write Byte Cycle – Single Error During Read Portion
- CSR 4 is set.
- Address and syndromes are NOT latched in CSR 5 through CSR 10.
- Bad data is corrected and combined with new byte.
- Check bits are generated by ECC on the new word.

Write Byte Cycle – Double Error During Read Portion
- CSR 15 is NOT set.
- Address and syndromes are not latched in the CSR. Error is preserved by writing the old data and check bits back into memory. The new byte is lost. Error is detected on the next DATI cycle to that location.

Write Word Cycle
- Check bits are generated by the ECC.
- Check bits and data are written into memory.

Check Bit Retrieval
The protected 16 kW block of memory stores the memory resident diagnostic. This block behaves as though it were in normal mode with ECC enabled. Check bits are not latched. The CSR stores check bits for the memory under test (not protected).

Inserting Check Bits
Check bits are not written from the CSR to the RAM check bits while in the protected block. This protected block behaves as though it were in normal mode with ECC enabled. Check bits are generated by the ECC.

4.3.3.8 Operating Modes Summary – Table 4-6 is a summary of error conditions in the seven operating modes when performing the various cycle types. As an example of how to use the table, assume the MSV11-J is in normal mode performing a write byte cycle and there is a single error. In this example, CSR 4 is set to 1, the error is corrected, address and syndrome bits are latched in the CSR, check bits are not latched and the source of the check bits is from the ECC in the data gate array.

Table 4-6 Error Condition Summary for Various Operating Modes

	Read			Write Byte		Write Word
	No Errors	Single Error	Double Error	No Errors	Single Error	Double Error
Normal Mode – ECC Enabled						
Error indication	–	CSR 4=1	CSR 15=1, LED	–	CSR 4=1	No	–
Error corrected	–	Yes	No	–	Yes	No	–
Latch address and syndrome	No	Yes	Yes	No	Yes	No	No
Latch check bits	No	No	No	No	No	No	No
Check bit source	MEM	MEM	MEM	ECC	ECC	MEM	ECC
Normal Mode – ECC Disabled						
Error indication	–	CSR 15, 4=1, LED	CSR 15=1, LED	–	CSR 15=1, 4=1, LED	No	–
Error corrected	–	No	No	–	Yes	No	–
Latch address and syndrome	No	Yes	Yes	No	Yes	No	No
Latch check bits	No	No	No	No	No	No	No
Check bit source	MEM	MEM	MEM	ECC	ECC	MEM	ECC
Protected Normal Mode – ECC Disabled						
Error indication	–	No	CSR 15=1, LED	–	No	No	–
Error corrected	–	Yes	No	–	Yes	No	–
Latch address and syndrome	No	No	Yes	No	No	No	No
Latch check bits	No	No	No	No	No	No	No
Check bit source	MEM	MEM	MEM	ECC	ECC	MEM	ECC
Diagnostic Mode – ECC Enabled						
Error indication	–	CSR 4=1	CSR 15=1, LED	–	No	No	–
Error corrected	–	Yes	No	–	Yes	No	–
Latch address and syndrome	No	No	No	No	No	No	No
Latch check bits	CSR	CSR	CSR	No	No	No	No
Check bit source	MEM	MEM	MEM	CSR	CSR	CSR	CSR

LED – Light emitting diode
ECC – Error correction logic
MEM – Memory
CSR – Control and status register

Table 4-6 Error Condition Summary for Various Operating Modes (Cont)

	Read			Write Byte			Write Word
	No Errors	**Single Error**	**Double Error**	**No Errors**	**Single Error**	**Double Error**	
Diagnostic mode – ECC Disabled							
Error indication	–	CSR 15, 4=1, LED	CSR 15=1, LED	–	No	No	–
Error corrected	–	No	No	–	Yes	No	–
Latch address and syndrome	No	No	No	No	No	No	No
Latch check bits	No	CSR	CSR	No	No	No	No
Check bit source	MEM	MEM	MEM	CSR	CSR	CSR	CSR
Protected Diagnostic Mode – ECC Enabled							
Error indication	–	CSR 4=1	CSR 15=1, LED	–	CSR 4=1	No	–
Error corrected	–	Yes	No	–	Yes	No	–
Latch address and syndrome	No	No	No	No	No	No	No
Latch check bits	No	No	No	No	No	No	No
Check bits source	MEM	MEM	MEM	ECC	ECC	MEM	ECC
Protected Diagnostic Mode – ECC Disabled							
Error indication	–	CSR 4=1	CSR 15=1, LED	–	CSR 4=1	No	–
Error corrected	–	Yes	No	–	Yes	No	–
Latch address and syndrome	No	No	No	No	No	No	No
Latch check bits	No	No	No	No	No	No	No
Check bit source	MEM	MEM	MEM	ECC	ECC	MEM	ECC

4.3.4 Error Reporting

During a PMI Read, a double word transfer occurs. The CSR must have a means of logging an error in either or both words.

All reads from memory are double word reads. The cycle type determines the number of words to be transmitted (i.e., one word during a Q-bus cycle, two words during a PMI cycle). Furthermore, the operating mode (i.e., normal, diagnostic mode) determines what is logged (i.e., check bits, syndrome bits).

The chart below shows the error logging for single and double word errors during PMI bus and Q-bus cycles. As an example of how to use the chart, assume there are two errors in the second word and no errors in first word during a PMI cycle. The second word is logged and CSR bit 15 is set. If a Q-bus cycle is executed under these conditions, no error logging occurs (Table 4-7).

Table 4-7 Error Logging

Number of Errors 2nd Word	1st Word	Double Word Transfer (PMI)	Single Word Transfer (Bus)
0	0	No log	No log
0	1	Log 1st, set CSR 04	Log 1st, set CSR 04
1	0	Log 2nd, set CSR 04	No log
1	1	Log 2nd, set CSR 04	Log 1st, set CSR 04
1	2	Log 1st, set CSR 04, 15	Log 1st, set CSR 15
0	2	Log 1st, set CSR 15	Log 1st, set CSR 15
2	0	Log 2nd, set CSR 15	No log
2	1	Log 2nd, set CSR 04, 15	Log 1st, set CSR 04
2	2	Log 2nd, set CSR 15	Log 1st, set CSR 15

NOTES:

1. *Log indicates that address and syndrome bits are latched when in normal operating mode. Refer to Paragraph 4.3.3 for details on the logging of errors for different operating modes and cycle types.*

2. *If it is desired to log the first word in normal mode error, during a PMI transfer the access sequence must be changed, i.e., first word must be accessed second. The reason for this is that the CSR bits for the first word are overwritten by the second word.*

3. *In diagnostic operating mode, check bits from the first word of a two word transfer are logged in the CSR. Check bits from the 2nd word are not logged. CSR 04 and CSR 15 will reflect the word with the most significant error.*

   As an example, during a PMI read, with no error in the first word and a double bit error in the second, the check bits from the first word will be latched in the CSR while the double bit error from the second word will set CSR 15 and turn on the red LED.

CHAPTER 5
DIAGNOSTICS

5.1 GENERAL
No maintenance is required for the MSV11-J.

CAUTION: All power must be off before installing or removing modules. Always be sure the component side of the memory faces in the same direction as the other modules within the LSI system.

5.2 PREVENTIVE MAINTENANCE
The MSV11-J requires no preventive maintenance, however, periodic preventive maintenance may be performed on the system. Consult the system manual for details.

1. Check the fans to be sure they operate when power is on.
2. Check air filters (if equipped).
3. Run diagnostic test if an operating problem is suspected.

5.3 DIAGNOSTIC TESTING

5.3.1 Introduction
The diagnostic test for the MSV11-J memory is CVMJA0 which is a standalone memory diagnostic. CVMJA0 is used to checkout ECC memories and/or parity memories. Running the CVMJA0 diagnostic destroys all the data stored in memory. In testing ECC memories, the diagnostic writes incorrect ECC data and verifies that the ECC logic is working correctly.

NOTE: In a PDP-11/84 UNIBUS system the diagnostic checks the Private Memory Interconnect (PMI) memory but does not check the UNIBUS memory.

5.3.2 Operational Switch Settings
The operational software switch settings and their functions are described in Table 5-1. To change the software switch register (SWR) contents, do a "CONTROL G" while the diagnostic is running. This causes a display of the current SWR value and the prompt for the octal input of the new SWR value from the terminal. This routine does not respond to CONTROL G if you have a hardware switch register.

In Table 5-1, the number in the second column is the octal value you type to select the particular SWR. For example, to select SWR 11 type 4000 (octal) which means that SWR 0 through 10 are 0's with SWR 11 being a 1. All other settings are 0's.

Example:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0		0			4			0			0			0	

Table 5-1 Switch Settings

Switch	Octal Value	Definition
0	1	Detect Single-bit Errors For manufacturing purposes this switch should always be on. For field service purposes this switch should always be off. This switch allows all ECC single-bit errors to be reported by disabling error correction. Error printouts of single-bit errors are not distinguished from double-bit errors.

NOTE: If double-bit errors are found in the memory, switch 0 should be set to make sure that new data can be written to the locations containing double-bit errors.

1-3 Test Mode
Test modes determine the recursion algorithm to be used during pattern test.

		Mode Name	Description
0	0	BAFPAF	Banks forward, patterns forward
1	2	BAFPAR	Banks forward, patterns reverse
2	4	BAWPAF	Banks worst first, patterns forward
3	6	BAWPAR	Banks worst first, patterns reversed
4	10	PAFBAF	Patterns forward, banks forward
5	12	PAFBAW	Patterns forward, banks worst first
6	14	PARBAF	Patterns reverse, banks forward
7	16	PARBAW	Patterns reverse, banks worst first

4	20	Fat Terminal This informs the program that the console terminal has a width of at least 132 columns.
5	40	Limit Max Errors Per Bank This limits the number of error typeouts per bank. The default is 10, however this can be changed by changing location "ERRMAX" manually.
6	100	Inhibit Configuration Map This inhibits the printing of a map showing the memory configuration.
7	200	Detailed Error Reports After any normal error report is typed, this option causes the contents of the following registers to be typed. R0, R1, R2, R3, R4, R5, SP, "CONTROL", "CPUERR"
8	400	Halt Program This initiates the following sequence. 1. If program is relocated it moves back to bank zero. 2. Flushs out all possible double-bit errors. 3. Turns off memory management. 4. Restores loaders. 5. Unmap the Unibus Map (if there is one).

Table 5-1 Switch Settings (Cont)

Switch	Octal Value	Definition
9	1000	Loop On Error This causes looping from failure point back to the last correctly initialized area of the current test.
10	2000	Bell On Error This causes a bell (or beep or click) on each error trap.
11	4000	Quick Verify If this switch is selected, about 1/64th of the possible combinations of single-bit errors and double-bit errors are tested.
12	10000	Inhibit Relocation This prevents the program from relocating and consequently prevents the program from testing at least 16Kwords of memory.
13	20000	Inhibit Error Typeouts This causes returns from the error routine without the typed messages. Other error functions are not effected.
14	40000	Loop On Test This causes looping on the present test or pattern (back to last scope trap). If in a pattern, then the looping is for an entire bank of 16K addresses.
15	100000	Halt On Error Continuing from this halt, the test first checks for a change in the software switch register ("Control G" in the TTY input buffer) then it continues testing.

5.3.3 CVMJA0 Diagnostic Operation

The following paragraphs list and describe three sample diagnostic printouts. The first example shows a complete sequence that includes power up, the booting sequence, and the diagnostic printout. This first example shows an error-free memory. The second example shows the diagnostic printout of a memory containing errors. The power up and booting sequence is similar to the first example and consequently is not shown. The third example shows the diagnostic printout of a non-contiguous memory. The power up and booting sequence is similar to the first example so it is not shown. The underlined text is typed in by the operator.

5.3.3.1 Example 1 – Error Free Printout

Power Up Test of KDJ11-B CPU

The following message appears each time the CPU is powered up.

```
Testing in progress -- Please wait
Memory Size is 4088 Kbytes
9 Step memory test
 Step 1 2 3 4 5 6 7 8 9

Message 04  Entering Dialog mode
```

Booting Up the System
To boot the system, type B DL0 and press return. Respond to the dialog that appears.

```
Commands are: [Help, Boot, List, Map, Test]
Type a command then press the RETURN key: B DL0 <CR>

Bootins DL0

Startins system

CHMDLB1 XXDP+ DL MONITOR 28K
BOOTED VIA UNIT 0

ENTER DATE (DD-MMM-YY) 31 OCT 84 <CR>

RESTART ADDR:153726
50 HZ? N <CR>

LSI? N <CR>

THIS IS XXDP+. TYPE 'H' OR 'H/L' FOR DETAILS
```

Running the CVMJA0 Diagnostic – The diagnostic printout and a description appears below.

```
.R CVMJA0 <CR>
  CVMJA0BIN
    CVMJA0  ECC/PARITY MEMORY DIAGNOSTIC
      11/83 CACHE AVAILABLE
  SWR = 000000  NEW =  <CR>


         CSR MAP

CSR        0 1 2 3 4 5 6 7 8 9 A B C D E F
MEMTYPE    E E

2044K OF MSV11-J
2044K WORDS OF MEMORY TOTAL
```

MEMORY CONFIGURATION MAP
16K WORD BANKS

```
                1       2       3       4       5       6       7
          01234567012345670123456701234567012345670123456701234567012345670123
ERRORS
MEMTYPE   EEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE
CSR       000000000000000000000000000000000000000000000000000000000000000000
PROTECT   PP

              1       1       1       1       1       1       1
              0       1       2       3       4       5       6
          45670123456701234567012345670123456701234567012345670123456701234567
ERRORS
MEMTYPE   EEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE
CSR       000011111111111111111111111111111111111111111111111111111111111111
PROTECT

          1
          7
          01234567
ERRORS
MEMTYPE   EEEEEEEE
CSR       11111111
PROTECT

END PASS #Q1
```

NOTES:

1. *The initial switch register setting is 000000. To enter a new switch register setting, refer to Paragraph 5.3.2.*

2. *The E in the MEMTYPE row designates ECC.*

3. *There is about two minutes running time after MEMTYPE appears in the CSR map. This time is required to size the memory and match the CSR to the memory. Actual time depends on the memory capacity and processor speed.*

4. *In the memory configuration map each column represents 16K word banks. The total memory consists of 167 banks octal. If all banks are filled, it represents two fully-populated MSV11-J memories for a total of two megawords (4 Mb) of memory. In this example, the 0s in the CSR row represent the first memory and the 1s represent the second memory.*

5. *The PROTECT PP directly below the row designated CSR indicates:*

   a. *Diagnostic is resident in one of two 16K word protected banks.*
   b. *The diagnostic cannot be destroyed because these two banks are protected.*
   c. *The two banks are alternately checked by relocating the diagnostic to the alternate bank.*

6. *END PASS #Q1 (end of pass completion) is a quick verify test. It runs about 15 minutes and checks only 1/64th of the possible combinations of single-bit errors and double-bit errors.*

To run the entire test routine, the user must enter Field Service mode. Type CONTROL F to enter this mode. An end of pass completion in this mode takes about 45 minutes.

Running time may vary, depending on memory size and speed of processor.

5.3.3.2 Example 2 – Printout Containing Memory Errors

This diagnostic printout contains errors in the upper half of memory (indicated by X's).

```
.R CVMJAO
CVMJAOBIN
 CVMJAO  ECC/PARITY MEMORY DIAGNOSTIC
   11/83 CACHE AVAILABLE
SWR = 000000  NEW = <CR>


                CSR MAP

CSR       0123456789ABCDEF
MEMTYPE   P E


  256K OF Q-BUS PARITY MEMORY
 1024K OF ECC MEMORY
 1280K WORDS OF MEMORY TOTAL

                    MEMORY CONFIGURATION MAP

                         16K WORD BANKS

                  1       2       3       4       5       6       7
          01234567012345670123456701234567012345670123456701234567012345670123
ERRORS                                                    XXXXXXXXXXXX
MEMTYPE   PPPPPPPPPPPPPPPPEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE
CSR       0000000000000000111111111111111111111111111111111111111111111111
PROTECT   PP

              1       1       1       1       1       1       1
              0       1       2       3       4       5       6
          45670123456701234567012345670123456701234567012345670123456701234567

ERRORS    XXXXXXXXXXXXXXXXXXX
MEMTYPE   EEEEEEEEEEEEEEEEEEE
CSR       11111111111111111111
PROTECT
```

NOTES:

1. *The P in the MEMTYPE row designates parity memory and the E designates ECC memory.*

2. *This example shows that the upper half of the ECC memory contains errors. Errors are indicated by the X's in columns 60 to 117 (octal). (See row labeled errors.)*

3. *The 0's in the CSR row denote the first memory (parity memory) and the 1's denote the second memory (ECC memory).*

5.3.3.3 Example 3 — Printout Showing Non-Contiguous Memory

```
.R CVMJA0
CVMJA0BIN
 CVMJA0  ECC/PARITY MEMORY DIAGNOSTIC
   11/83 CACHE AVAILABLE
SWR = 000000  NEW = <CR>


                CSR MAP

CSR       0123456789ABCDEF
MEMTYPE   P E

  256K OF Q-BUS PARITY MEMORY
 1024K OF ECC MEMORY
 1280K WORDS OF MEMORY TOTAL

                    MEMORY CONFIGURATION MAP

                         16K WORD BANKS

                1       2       3       4       5       6       7
          01234567012345670123456701234567012345670123456701234567012345670123
ERRORS
MEMTYPE   PPPPPPPPPPPPPPPP                EEEEEEEEEEEEEEEEEEEEEEEEEEEE
CSR       0000000000000000                1111111111111111111111111111
PROTECT   PP

                1       1       1       1       1       1       1
                0       1       2       3       4       5       6
          45670123456701234567012345670123456701234567012345670123456701234567
ERRORS
MEMTYPE   EEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEEE
CSR       1111111111111111111111111111111111111111
PROTECT
```

NOTES:

1. *The 0's in the CSR row denote first memory (parity memory) and the 1's denote second memory (ECC memory).*

2. *There is a non-contiguous area from 20 to 37 (octal). Indicated by blank spaces.*

3. *The example represents the MSV11-P loaded with starting address 0 and the MSV11-J with starting address 0.5 Megawords (1MB).*

   The memory can be made contiguous by changing the starting address switch setting of the MSV11-J memory.

5.4 DIGITAL'S SERVICES

Maintenance can be performed by the user or by Digital. Digital's maintenance and on-site services are described in Chapter 1 of the Microcomputer Processor Handbook (EB-18451-20).

5.4.1 Digital Repair Service

Digital Field Service offers a range of flexible service plans.

ON-SITE SERVICE offers the convenience of service at your site and insurance against unplanned repair bills. For a small monthly fee you receive personal service from our Service Specialist. Within a few hours the specialist is dispatched to your site with equipment and parts to give you fast and dependable maintenance.

BASIC SERVICE offers full coverage from 8 a.m. to 5 p.m., Monday through Friday. Options are available to extend your coverage to 12-, 16-, or 24-, hour days, and to Saturdays, Sundays, and holidays.

DECservice offers a premium on-site service that guarantees extra-fast response and nonstop remedial maintenance. We don't leave until the problem is solved, which makes this service contract ideal for those who need uninterrupted operations.

Under Basic Service and DECservice all parts, materials, and labor are covered in full.

CARRY-IN SERVICE offers fast, personalized response, and the ability to plan your maintenance costs for a smaller monthly fee than On-Site Service. When you bring your unit to one of 160 Digital Servicenters worldwide, factory-trained personnel repair your unit within two days (usually 24 hours). This service is available on selected terminals and systems. Contact your local Digital Field Service Office to see if this service is available for your unit.

Digital Servicenters are open during normal business hours, Monday through Friday.

DECmailer offers expert repair at a per use charge. This service is for users who have the technical resources to troubleshoot, identify, and isolate the module causing the problem. Mail the faulty module to our Customer Returns Center where the module is repaired and a replacement is mailed back to you within five days.

PER CALL SERVICE offers a maintenance program on a noncontractual, time-and-material-cost basis. This service is available with either On-Site or Carry-In Service. It is appropriate for customers who have the expertise to perform first-line maintenance, but may occasionally need in-depth support from Field Service.

Per Call Service is also offered as a supplementary program for Basic Service customers who need maintenance beyond their contracted coverage hours. There is no material charge in this case.

On-Site Per Call Service is provided on a best effort basis, with a normal response time of two to three days. It is available 24 hours a day, seven days a week.

Carry-In Per Call Service is available during normal business hours, with a two to three day turnaround.

Digital International Field Service Information Numbers

U.S.A.	1-(800)-554-3333	Denmark	430-1005
Canada	(800)-267-5251	Spain	91-7334370
United Kingdom	(0256)-57122	Finland	90-423332
Belgium	(02)-242-6790	Holland	(01820)-34144
West Germany	(089)-9591-6644	Switzerland	01-8105184
Italy	(02)-617-5381/2	Sweden	08-987350
Japan	(03)-989-7161	Norway	2-256422
France	1-6873152		

INDEX

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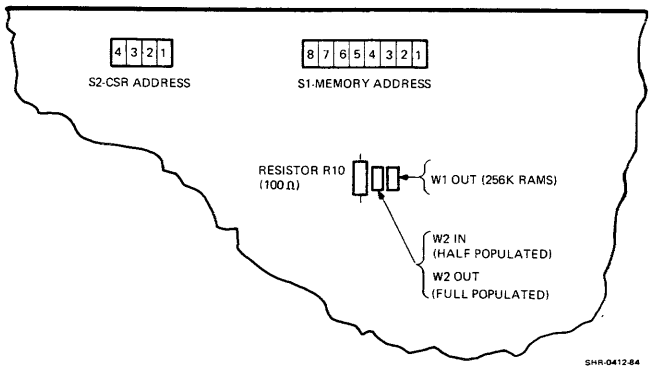


MEMORY STARTING ADDRESS

Memory Address Switch	Equivalent Starting Address
1	1 MW (2Mb)
2	512 kW (1Mb)
3	256 kW (512 kb)
4	128 kW (256 kb)
5	64 kW (128 kb)
6	32 kW (64 kb)
7	16 kW (32 kb)
8	8 kW (16 kb)

Example: 0 kW Starting Address
SW1 through SW8 Off
Example: 96 kW Starting Address
SW5 and SW6 = On, all others Off

CSR ADDRESS

Address	Switch Settings 1	2	3	4
17772100	Off	Off	Off	Off
17772102	Off	Off	Off	On
17772104	Off	Off	On	Off
17772134	On	On	On	Off
17772136	On	On	On	On

Example: CSR Address = 17772106
Switches 3 and 4 On
Switches 1 and 2 Off

digital™

EK-MSV1J-HR-001

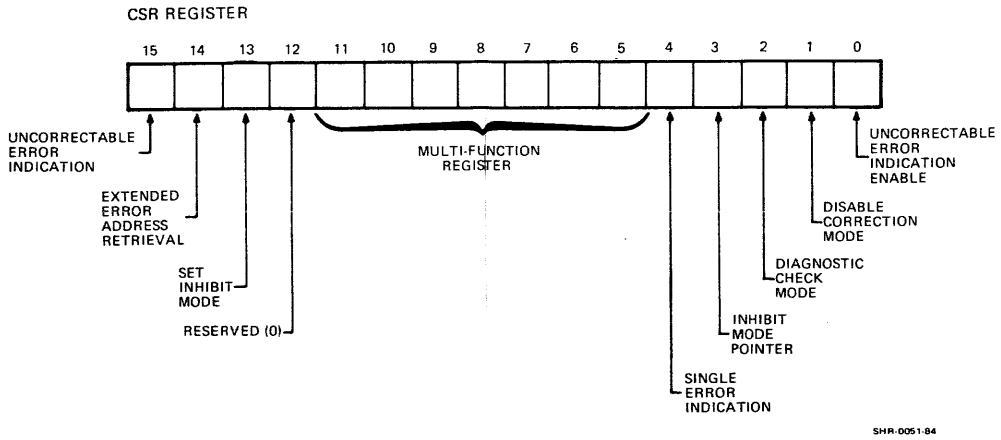
MSV11-J CONFIGURATION SUMMARY

MSV11-J is a metal oxide semiconductor, random access memory. It uses error detection and correction (ECC), a control and status register (CSR) to store status and error information, and has starting addresses on 8 kW boundaries. The board can be configured half or fully populated with 256K dynamic RAMs. Maximum memory capacity 2 Mb.

The memory is for Q-bus systems and supports the private memory interconnect (PMI) protocol of the KDJ11-B processor. The PMI bus is specifically designed for and used in the PDP-11/83 Q-Bus System and the PDP-11/84 UNIBUS System.

MSV11-J memory has these features.

- Has starting addresses on 8 kW boundaries
- Uses 256K dynamic RAMs. Board can be full or half populated
- Executes normal Q-bus protocol and faster PMI protocol
- Uses two gate arrays (VLSI technology) and advanced Schottky TTL logic
- Battery backup can be configured on board
- Green LED indicator on module indicates the presence of +5 volts (+5 VBB when configured for battery backup)
- On board refresh of the RAMs is transparent to CPU
- Compatible with 18- or 22-bit address backplane
- Error correction logic (ECC) to detect and correct single-bit errors and to detect double-bit errors
- Red LED indicator on module to indicate the detection of an uncorrectable error
- Contains CSR which can be assigned one of 16 addresses
- ECC operation can be controlled via CSR
- CSR operating modes facilitate diagnostic testing
- Memory compatible with Q-CD backplanes **(not compatible with Q-Q backplane).**



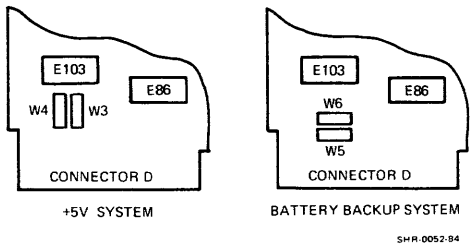
CSR15 = 0 No uncorrectable error detected
= 1 Uncorrectable error detected
CSR14 = 0 A11 through A17 to CSR11–CSR05
= 1 A18 through A21 and A01 to CSR05–CSR09
CSR13 = 0 Clear Inhibit Mode
= 1 Set Inhibit Mode
CSR12 = Reserved (always 0)
CSR11–CSR05 = Log address and syndrome bits in Normal Mode and checkbits in Diagnostic Mode

CSR04 = 0 No single error detected
= 1 Single error detected
CSR03 = 0 0–16 kW ECC Protect
= 1 16 kW–32 kW ECC Protect
Note: CSR13 must be set for CSR03 to function
CSR02 = 0 Normal Operation
= 1 Diagnostic Mode
CSR01 = 0 Enable Error Correction
= 1 Disable Error Correction
CSR00 = 0 Inhibit Error Indication
= 1 Active Error Indication

OPERATING MODES

		CSR Bits							
		15	14	13	4	3	2	1	0
1	Normal	X	X	X	X	X	0	0	X
2	Diagnostic	X	X	0	X	X	1	0	X
3	Diagnostic, Protected	X	X	1	X	X	1	0	X
4	ECC Disable	X	X	0	X	X	0	1	X
5	ECC Disable, Protected	X	X	1	X	X	0	1	X
6	Diagnostic, ECC Disable	X	X	0	X	X	1	1	X
7	Diagnostic, Disable, Protected	X	X	1	X	X	1	1	X

X = don't care



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