Part Number 30040-1

MODEL DQ614
DISC CONTROLLER
INSTRUCTION MANUAL

March 1984

DISTRIBUTED LOGIC CORP.
DILOG

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DESCRIPTION

INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ614 Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to ST506 compatible Winchester disc drives. The complete controller occupies one dual-wide module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is software compatible with DEC drivers, emulating RL01/RL02 drives.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is done automatically each time power is applied or under operator control by pressing the RESET switch. A green diagnostic indicator on the controller board lights if self-test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. An error correction code (ECC) with a 32-bit checkword corrects error bursts up to 11 bits. To compensate for media errors, bad sectors are skipped and alternates assigned, and there is an automatic retry feature for read errors. The controller is capable of addressing two megawords and controlling up to two disc drives in various configurations up to a total on-line capacity of 40 megabytes. Figure 1-1 is a simplified diagram of a disc system.

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q bus interface lines are listed in Table 1-1.

*DEC is a registered trademark of Digital Equipment Corporation.

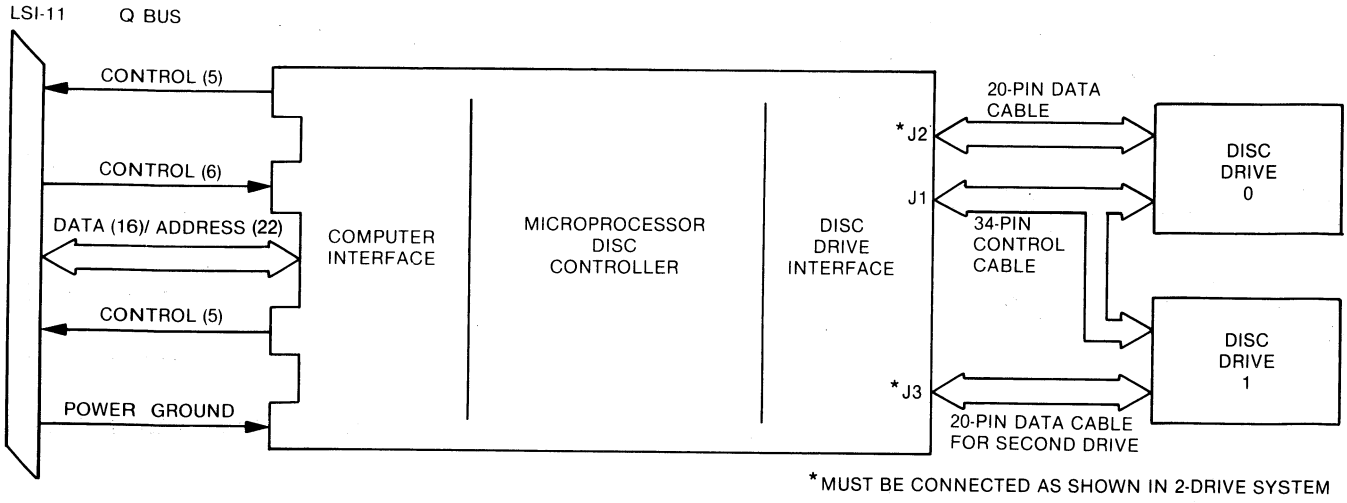


Figure 1-1. Disc Controller System Simplified Diagram

Table 1-1. Controller/Q-Bus Interface Lines

BUS PIN	MNEMONIC	INPUT/ OUTPUT	DESCRIPTION
AJ1, AM1, RT1, BJ1, BM1, BT1, BC2, CJ1, CM1, CT1, CC2, DJ1, DM1, DT1, DC2	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.
BA1	BDCOK H	I	DC power ok. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power ok. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	N/A	External Event Interrupt Request.
BV1, AA2, BA2, CA2, DA2	+5	I	+5 volt system power.
AD2, BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AL2	BIRQ L	O	Interrupt Request.
AM2 AN2 CM2 CN2	BIAK1I L BIAK1O L BIAK2I L BIAK2O L	I O I O	Serial Interrupt Acknowledge input and output lines routed from Q-Bus, through devices, and back to processor to establish and interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2, AV2, BE2, BF2, BH2, BJ2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2	BDAL0 L through BDAL15 L	I/O	Data/address lines, 0-15.
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I	DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1, AD1, BC1, BD1, BE1, BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21

INTERRUPT

The interrupt vector address is factory set to address 160. The vector address is programmed in a PROM on the controller, allowing user selection.

Interrupt requests are generated under the following conditions:

1. A hard error occurs.
2. A soft error occurs. Soft errors are checksum errors (CSE).

3. The designated number of words has been transferred.
4. A selected disc drive has accepted a seek or drive reset command.
5. A seek or drive reset function has been completed.

DISC INTERFACE

The controller interfaces with one or two disc drives through 34- and 20-pin cables. If two drives are used, the 34-pin control cable is daisy chained to drive 0 and 1. The 20-pin data cables are connected separately from the controller to each drive. The maximum cable length is 20 feet. Table 1-2 lists the control interface signals. Table 1-3 lists the data interface signals.

OPERATING SYSTEM COMPATIBILITY

RT11: The emulation is transparent to the RT11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSX11*: The emulation is transparent to the RSX11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSTS*: The emulation is transparent to the RSTS version 7.1 operating system, using the standarad device handler supplied by DEC.

CONTROLLER SPECIFICATIONS†

- Mechanical — The DQ614 is completely contained on one dual module 8.62 inches high by 5.19 inches wide and plugs into and requires one dual slot in any DEC LSI-11 backplane.
- Computer I/O—
  Register Addresses (PROM selectable)
  - Control/Status Register (RLCS) 774 400
  - Bus Address Register (RLBA) 774 402
  - Disc Address Register (RLDA) 774 404
  - Multipurpose Register (RLMP) 774 406
  - Address Extension Register (RLAE) 774 410
- Data Transfer
  - Method: DMA
  - Maximum block size transferred in a single operation is 16K words.
- Bus Load
  - 1 std unit load
- Address Ranges
  - Computer Memory: to 2 megawords
- Interrupt Vector—Four interrupt levels jumper selectable. Factory set to Address 160, level 5.

*RSX and RSTS are registered trademarks of Digital Equipment Corporation.

Table 1-2. Controller To Drive I/O Interface — "A" Cable

Signal Name (DILOG Term)	Pin	Source
Ground	1	
REDUCE WRITE CURRENT (REDUCE I)	2	Controller
Ground	3	
HEAD SELECT 3 (HESL3)	4	Controller
Ground	5	
WRITE GATE	6	Controller
Ground	7	
SEEK COMPLETE (SEEK COMP)	8	Drive
Ground	9	
TRACK 0	10	Drive
Ground	11	
WRITE FAULT (FAULT)	12	Drive
Ground	13	
HEAD SELECT 1 (HESL1)	14	Controller
Ground	15	
SELECT/NOT USED	16	Drive
Ground	17	
HEAD SELECT 2 (HESL2)	18	Controller
Ground	19	
INDEX	20	Drive
Ground	21	
READY	22	Drive
Ground	23	
STEP	24	Controller
Ground	25	
DRIVE SELECT 1 (DRSL1)	26	Controller
Ground	27	
DRIVE SELECT 2 (DRSL2)	28	Controller
Ground	29	
DRIVE SELECT 3 (DRSL3)	30	Controller
Ground	31	
NOT USED	32	
Ground	33	
DIRECTION IN	34	Controller

- Disc Drive I/O
  - Connector—One 34-pin flat ribbon cable and two 20-pin flat ribbon cables.
- Signal: ST506 compatible
- Power: +5 volts @ 3.5 amps (typical), +12 volts at 300 milliamps from computer power supply.
- Environment: Operating temperature 0 °C to 45 °C., humidity 0 to 70% non-condensing.
- Shipping Weight: 5 pounds including documentation and cables.
- Shock—Non-repetitive of less than 0.5G.

†Specifications subject to change without notice.

Table 1-3. Controller to Drive Data Cable — "B" Cable

Signal	Pin	J2 Term	J3 Term	Source
DRIVE SELECTED	1	DRIVE SELECTED UNIT 0	DRIVE SELECTED UNIT 1	Drive
Ground	2	—	—	—
Reserved	3	—	—	—
Ground	4	—	—	—
Reserved	5	—	—	—
Ground	6	—	—	—
Reserved	7	—	—	—
Ground	8	—	—	—
Reserved	9	—	—	—
Spare	10	—	—	—
Ground	11	—	—	—
Ground	12			
WRITE DATA +	13	WDAT0 +	WDAT1 +	Controller
WRITE DATA –	14	WDAT0 –	WDAT1 –	Controller
Ground	15	—	—	—
Ground	16	—	—	—
READ DATA +	17	RDAT0 +	RDAT1 +	Drive
READ DATA –	18	RDAT0 –	RDAT1 –	Drive
Ground	19	—	—	—
Ground	20	—	—	—

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and may contain cables if this option is exercised. The controller is completely contained on the dual-size printed circuit board. Disc drives, if supplied, are contained in separate shipping cartons. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller. Table 2-1 lists the configuration switch setting, and Table 2-2 lists component and jumper options. Ensure the board is properly configured before installing.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

NOTE

The controller may be inserted into any A-B connector slot, all of which are Q-bus slots. On some backplanes, C-D slots may be Q-bus slots or may be interconnect slots. Before inserting the controller in any C-D slot, check the appropriate DEC documentation.

There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option boards, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 × N2	C0 × M2	BIAK1/L0
C0 × S2	C0 × R2	BDMG1/L0
↑ Last Full Option Slot	↑ Controller Slot	

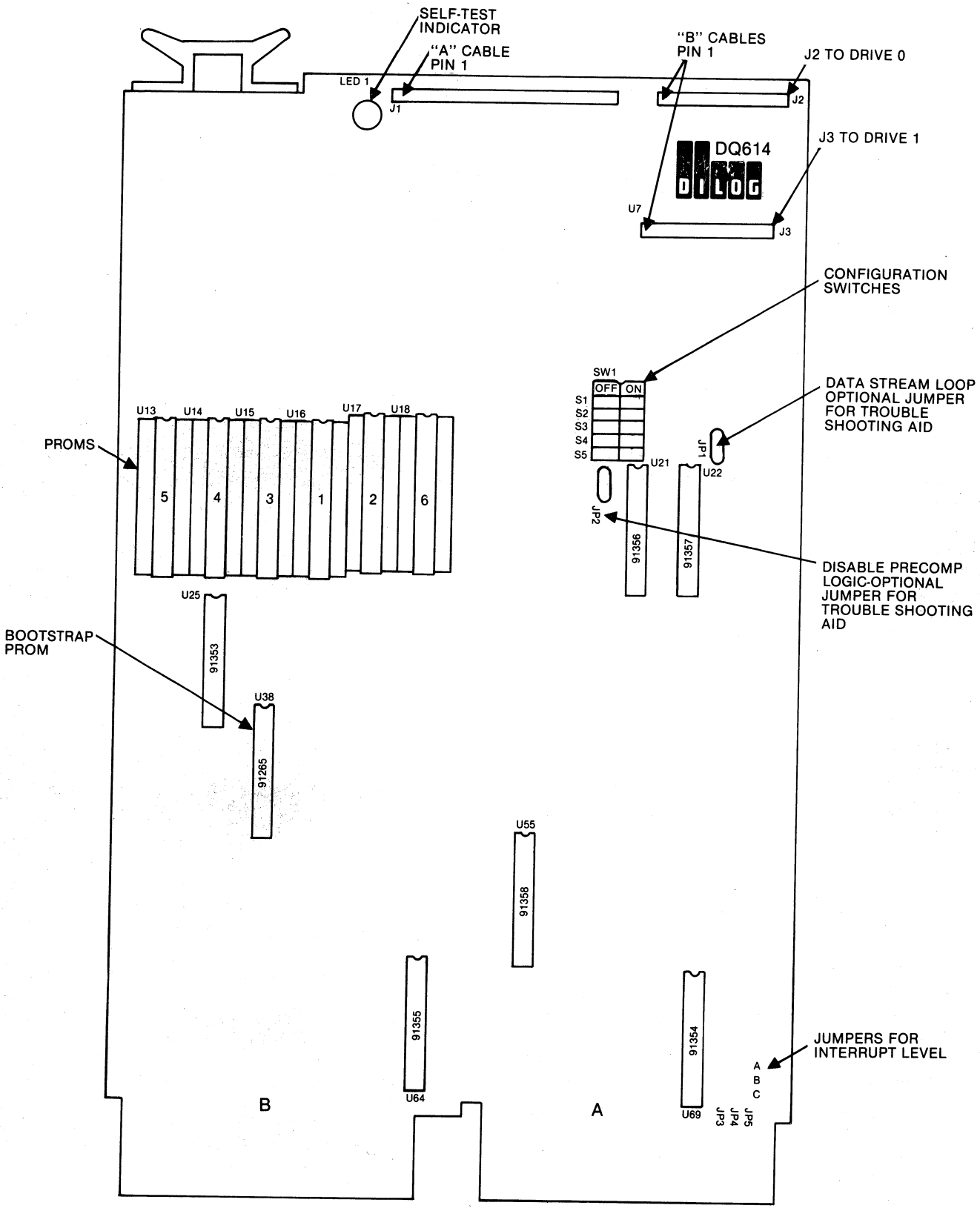


Figure 2-1. Controller Configuration

Table 2-1. Configuration Switches

SWITCH	POSITION	DESCRIPTION
S1	ON	The ECC syndrome is saved during a read operation. Upon detection of an error, the controller can use the syndrome to determine if the error is correctable. If correctable, the controller will transparently correct the error.
	OFF	The ECC syndrome is discarded during a read operation. Upon detection of an error, the controller will determine that the error is uncorrectable (because of the lack of proper syndrome). This mode should be used by the operator when running diagnostics, so that all media flaws can be detected and mapped out.
S2	ON	Controller bootstrap enabled.
	OFF	Controller bootstrap disabled.
S3, S4		Identify, to the microprocessor, the last logical RL unit that exists on physical drive zero: **SW3 SW4 PHYSICAL ZERO PHYSICAL ONE** OFF OFF DL0 DL1, DL2, DL3 OFF ON DL0, DL1 DL2, DL3 ON OFF DL0, DL1, DL2 DL3 ON ON DL0, DL1, DL2, DL3
S5	ON	Controller assumes alternate address for bootstrap ROM of 175 000. (Must be used for LSI 11/23 plus CPU, module M8189.)
	OFF	Controller assumes primary address for bootstrap ROM of 173 000
When shipped from the factory, all switches will be off if the order is for a controller only. If the order is for drive integration, the switches will be set for that configuration.		

Table 2-2. Component and Jumper Options

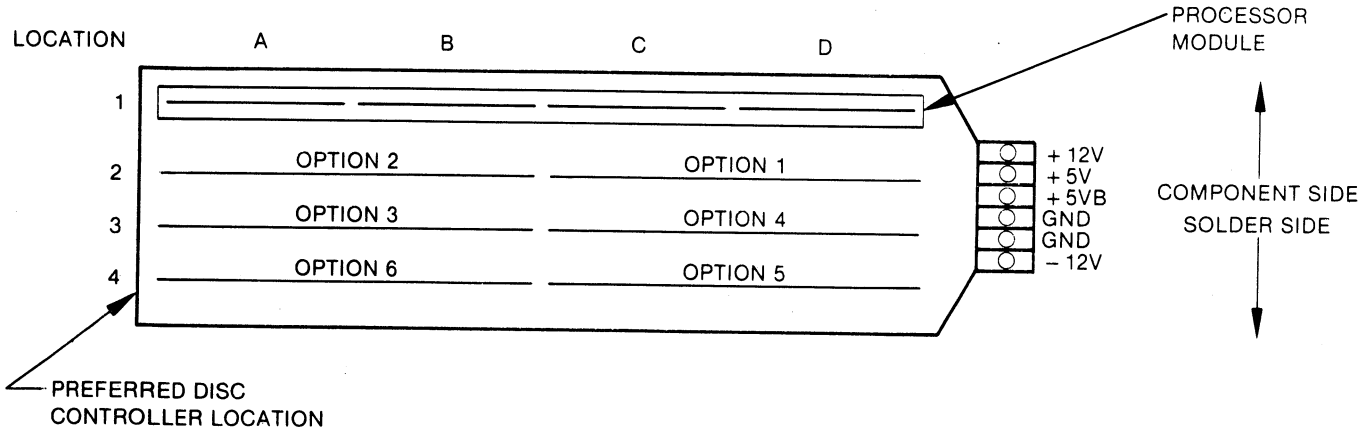
OPTION	LOCATION	DESCRIPTION
Special Bootstrap*	U38	PROM—allows the user to incorporate bootstrap programs not supported by DILOG.
Loop back data stream	U22-U23	JP1—Jumper removed (etch cut) forces the write logic to create a data stream which can be looped back into the read logic. Troubleshooting aid.
Abort Precompensation	U32	JP2—Jumper removed (etch cut) aborts the controller precompensation logic when writing data. Troubleshooting aid.
Interrupt Level	U70	JP3, JP4, JP5—This option consists of cutting etches and installing wires. For the interrupt levels, the jumpers are connected as follows: JP3 JP4 JP5 Interrupt Level 4 B-C B-C B-C Interrupt Level 5 B-C B-C A-B Interrupt Level 6 B-C A-B B-C Interrupt Level 7 A-B A-B B-C
Drive 0 Cartridge Changed	JP6 (U22)	Must be removed.
Drive 1 Cartridge Changed	JP7 (U22)	Must be removed.
Enable Sector Pulse	JP8 (U5)	Must be removed.
Enable Switches 3 and 4	JP9 (U32)	Must be installed.
Read Postamble	JP (U32)	**JUMPER** A-B Must be installed A-C Must be removed
*If the special bootstrap option is required, the sales order should indicate this. The loop back data stream and abort precompensation will not have the etch cut when shipped. The interrupt level shipped from the factory is Level 5, Address 160.		

2. To the controller connectors, install cables J1, J2, and J3, respectively. Ensure the pin 1's are oriented as shown in the illustration.

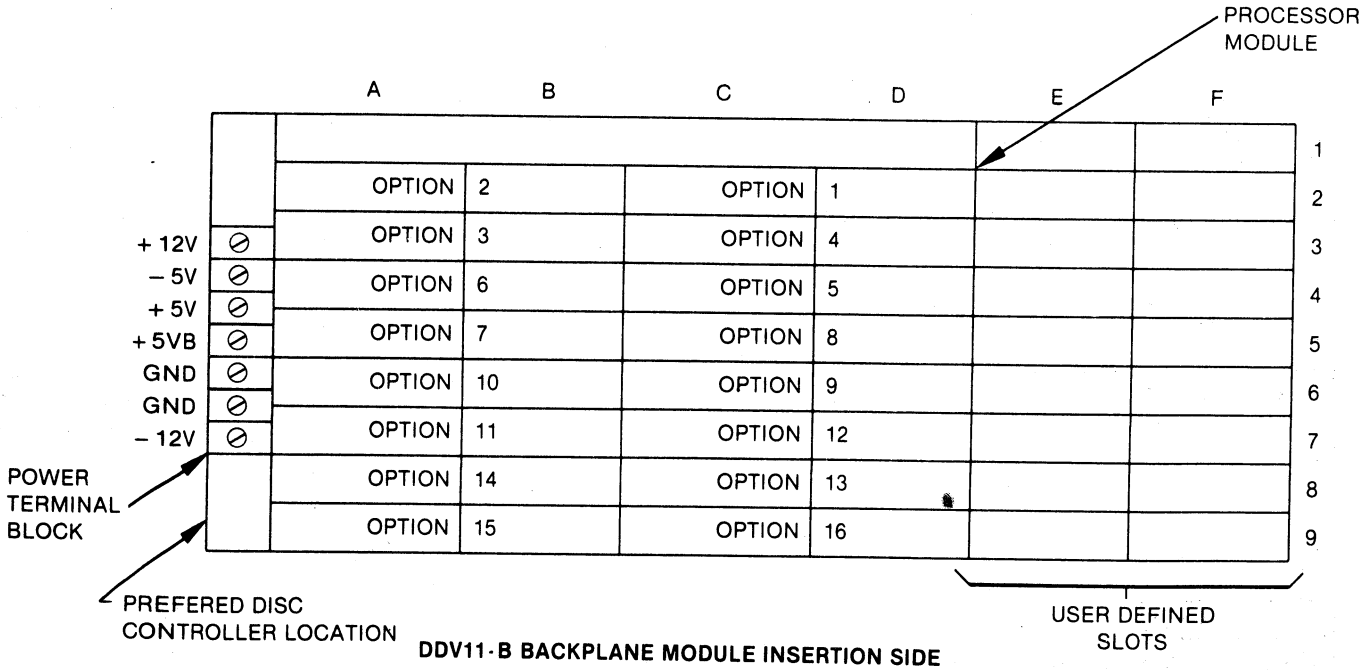
Note

It may be necessary to remove the strain relief bar on the J3 cable to install the connector.

3. Gently position the module slot connectors into the backplane and press until the connectors are firmly seated into the backplane. Apply equal pressure to both sides of the controller when installing or removing.
4. Route the cables to the drive; assure pins are properly aligned; and connect the cables. Ensure that the bus terminator is installed in the last drive in the system.
5. Refer to the disc drive manual, the computer manual, and Section 3 of this manual, for operating instructions.



H9270 MODULE INSERTION SIDE



DDV11-B BACKPLANE MODULE INSERTION SIDE

NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

SECTION 3
OPERATION

INTRODUCTION

This section contains procedures for operating the computer system with the controller and a disc drive or drives. An understanding of DEC operating procedures is assumed.

PRECAUTIONS AND PREOPERATIONAL CHECKS

The following precautions should be observed while operating the system. Failure to observe these precautions could damage the controller, the disc, the computer, or could erase a portion or all of the stored software.

1. Ensure all switches listed in Table 2-1 are properly set.
2. Ensure all jumpers listed in Table 2-2 are properly installed.
3. Verify that the controller board is firmly seated in the backplane connection.
4. Verify that the cables are properly installed in the controller and in the disc drive.
5. Apply power to the drive, the computer and the terminal.
6. Verify that the green diagnostic LED on the edge of the controller board lights.

BOOTSTRAP SWITCHES

When switch 2 is on (closed), the controller bootstrap is enabled. The DILOG program will boot the system for RL01/RL02 or RX02 Floppy disc dual density. When switch 2 is off (open), the bootstrap is disabled, and the controller will boot from the standard DEC REV-11 module.

When switch 5 is on (closed), the controller will assume the alternate address 175000 for the bootstrap ROM. When switch 5 is off (open), the controller will assume the primary address 173000 for the boostrap ROM

Note

If a system has more than one device with bootstrap capabilities enabled, the bootstraps must be at different addresses.

BOOTSTRAP PROCEDURE

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate DEC manual for a discussion of the Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

@ 173000G or 175000G

Depends on switch and jumper configuration above.

* Respond for appropriate logical unit with DY0 or DY1 <CR> for RX02 or DL0, DL1, DL2 or DL3 <CR> if RL01/RL02.

FORMAT AND TEST PROGRAMS

To format the disc, the operator identifies the drive type, the emulation (RL01 or RL02) and the alternate cylinders required, and the program basically does the rest. For testing, the operator identifies the test and the unit, and the program exercises the system.

To run the program, load the medium and enter R DQ614 after the program is loaded. The following will appear:

ARE YOU RUNNING THE DIAGNOSTIC VIA A CRT. (Y OR N)?

ENTER NUMBER OF DRIVES ON SUB-SYSTEM (1 OR 2)?

If the answer to the first question is no, the program will not list current cylinder addresses (a printout, for example, would be too extensive). To the second question, answer 1 or 2. The disc drive menu will appear next listing a sequential number, the name of the manufacturer and the model number. The following will also appear:

XXX DRIVE (0 or 1) XXX

ENTER THE NUMBER CORRESPONDING TO THE DISC DRIVE.

OR

SELECT ANOTHER PAGE

N = NEXT PAGE P = PREVIOUS PAGE
E=DRIVE NOT FOUND

The number to be entered is the sequence number on the list not the model number. Manufacturers and models are listed below. Select the next page of the menu by pressing N or the previous page by pressing P.

If the drive to be formatted is not listed in the menu, press E and the following will appear:

ENTER NUMBER OF HEADS (D)

ENTER NUMBER OF CYLINDERS(D)

REDUCE WRITE CURRENT AT CYLINDER (NOT USED) Default <CR>

START PRECOMPENSATION AT CYLINDER (NOT USED)

ENTER NUMBER CORRESPONDING TO PROPER STEP RATE:

1 = 26 US
2 = 280 US
3 = 2.1 MS
4 = 3.0 MS

The information above is taken from the manufacturer's specifications. Head and cylinder number are entered in decimal (D). Write current and precompensation requests do not require responses for all drives. If no response is required, press the carriage return for an answer. For the step rate, enter the sequence number and not the timing value.

After the drive is selected, the disc configuration will be selected:

DISC CONFIGURATION XXX DRIVE 0 XXX

ENTER NUMBER CORRESPONDING TO THE TYPE OF RL UNIT

1 = RL01 (10240 Blocks; XXX CYLINDERS)
2 = RL02 (20480 Blocks; XXX CYLINDERS)
(XXX) = CYLINDERS NOT YET ALLOCATED

YOU HAVE XXX CYLINDERS

USE THE <TAB> TO ENTER TYPE OF RL UNIT

CARRIAGE RETURN COMPLETES CONFIGURATION PROCEDURE

DL0: ( ) DL1: ( ) DL2: ( ) DL3:

Use the tab when entering the type of RL unit (1 or 2). Use the carriage return to exit after a physical drive is partitioned. The program will automatically calculate the number of cylinders remaining after the selection of the RL unit. The operator has the option of selecting a truncated unit or allocating the remaining cylinders as alternates, or a combination of both. If the remainder is less than 1 megabyte, the program automatically allocates the remainder as alternates. The alternate cylinders that are allocated are for the physical drive and not the logical unit. The operator allocates the alternate cylinders and the program calculates and allocates the truncated unit. The following is an example:

The first logical unit is to be an RL01 and there are 65 cylinders remaining, 5 of which are to be alternates and 60 truncated. The following underlined numbers or keys are entered:

DL0: 1<TAB> (65) DL1: <CR>
( )DL2: ( ) DL3:

ENTER NUMBER OF ALTERNATE CYLINDERS (D)? 5 <CR>

Note

If there is no tab on the terminal, use control I.

If two drives are selected, the cursor may appear at DL1, DL2, or DL3, depending upon how many logical units are selected. In the previous example, if two drives are selected, the cursor will be positioned at DL2.

A truncated unit of 60 cylinders will appear in DL1. The following will appear:

DL0: 1 (65) DL1: ( ) DL2: ( ) DL3:

When all logical units are partitioned, the summation message will be similar to the following:

DISC SUBSYSTEM CONFIGURATION

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DL0	0	10.48	20480
DL1	0	4.17	8160
DL2	1	5.24	10240
DL3	1	5.24	10240

PHYSICAL DRIVE 0 HAS 30 ALTERNATE TRACKS

PHYSICAL DRIVE 1 HAS 54 ALTERNATE TRACKS

SET SWITCH 3 OFF
SET SWITCH 4 ON

ARE YOU SURE (Y OR N)?

Partitioning is then completed.

The following is a partial list of manufacturers and model numbers that can be formatted:

1. AMPEX PYXIS 8
2. AMPEX PYXIS 13
3. AMPEX PYXIS 16
4. AMPEX PYXIS 20
5. AMPEX PYXIS 27
6. COMPUTER MEMORIES CMI-5410
7. CMI 5412
8. CMI 5616
9. CMI 5619
10. CMI 5640
11. EVOTEK ET-5510
12. ET-5520
13. ET-5530
14. ET-5540
15. FUJITSU M2231A
16. FUJITSU M2232A
17. INTERNATIONAL MEMORIES IMI-5006
18. IMI-5006H
19. IMI-5012H
20. IMI-5018H

21. MINISCRIBE 1006
22. MINISCRIBE 1012
23. MINISCRIBE 3006
24. MINISCRIBE 3010
25. MINISCRIBE 4010
26. MINISCRIBE 4020
27. MITSUBISHI 4861
28. MITSUBISHI 4862
29. MITSUBISHI 4863
30. OLIVETTI HD562/11
31. RODIME 102
32. RODIME 104
33. RODIME 202
34. RODIME 203
35. RODIME 204
36. RODIME 206
37. RODIME 208
38. RMS/DISCTRON 503
39. RMS/DISCTRON 504
40. RMS/DISCTRON 506
41. RMS/DISCTRON 509
42. RMS/DISCTRON 512
43. RMS/DISCTRON 513
44. RMS/DISCTRON 514
45. RMS/DISCTRON 518
46. RMS/DISCTRON 519
47. RMS/DISCTRON 526
48. SEAGATE ST406
49. SEAGATE ST412
50. SEAGATE ST419
51. SEAGATE ST506
52. SHUGART SA602
53. SHUGART SA604
54. SHUGART SA606
55. SYQUEST SO306
56. TANDON 602E
57. TANDON 602S
58. TANDON 603E
59. TANDON 603S
60. TEXAS INSTRUMENTS TI-506
61. TI-525/61
62. TI-525/122
63. ATASI 3020
64. ATASI 3033
65. ATASI 3046
66. OLIVETTI HD562/13
67. MEMOREX 306
68. MEMOREX 310

DIAGNOSTIC TEST PROGRAM

The format/test program contains the following:

1. TEST CONTROLLER
   A. Registers
   B. Data Buffer
2. TEST DISC DRIVE
   A. Disc Ready
   B. Disc Restore (seek to cylinder 0)
3. FORMAT
   A. Write Headers
   B. Read Headers
   C. Write Data Test Pattern
   D. Read Data Test Pattern
4. SEQUENTIAL READ
5. SELECTED READ
6. RANDOM SEEK, READ
7. RANDOM SEEK, WRITE, READ, AND COMPARE
8. TEST ECC LOGIC
9. ASSIGN ALTERNATE TRACK

Test Controller

The program will automatically test the controller registers and data buffer. The program will only display error messages during this test; the display will be:

DATA BUFFER ERROR

or the mnemonics of the seven controller registers, the location and contents (in Octal). The display of the registers is followed by a 4-line message to aid in isolating the specific problem.

Note

Whenever an error occurs and the registers are displayed, an audio alarm signal is generated to notify the operator.

The 4-line message is as follows:

DISC ADDRESS _____ HEAD _____
CYLINDER _____
TYPE OF COMMAND _____
CONTROL STATUS ERROR _____
DRIVE STATUS _____

"DISC" lists the head and cylinder (in decimal) where the error occurred. An example of Type of Command is Read Data Command. An example of Control Status is Seek Error. The Drive Status will display:

USE C TO CONTINUE
USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

"C" is used to continue the test. "O" is used for ODT (on-line debugging technique), "L" is used to initiate the system bootstrap.

Test Disc Drive

After the controller test is performed, the program will automatically test the drive for ready and restore. The disc address is not displayed during this test.

Format

The operator may either select logical units sequentially or select one or more specific logical units to be formatted. Program messages are presented for formatting in logical unit number sequence, i.e.:

FORMAT DL0 (Y OR N)?
FORMAT DL1 (Y OR N)?
FORMAT DL2 (Y OR N)?
FORMAT DL3 (Y OR N)?
FORMAT ALTERNATE CYLINDERS (DRIVE 0 OR DRIVE 1)

Note

Before any write operation, the program will display ARE YOU SURE? This aids the operator in preventing reformatting of a previously formatted logical unit (possibly destroying good data).

During formatting, the following messages will appear sequentially:

WRITING HEADERS
CURRENT CYLINDER ADDRESS _____

READING HEADERS
CURRENT CYLINDER ADDRESS _____

WRITING DATA TEST PATTERN _____
CURRENT CYLINDER ADDRESS _____

READING DATA TEST PATTERN _____
CURRENT CYLINDER ADDRESS _____

When reading and writing headers, the program will display the cylinder addresses sequentially. The test pattern tests are also sequentially selected, and the cylinder address displayed will correspond to current address being read.

After each logical unit is formatted, the display will be:

DL____ FORMAT AND VERIFICATION COMPLETE

Sequential Read

For this test, the display will be:

SEQUENTIAL READ (ALL CYLINDERS AND HEADS?)

If the response is No, the program will jump to the Selected Read test. If the response is Yes, the current cylinder address is displayed as each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message, and the following:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK?

If no alternates (spares) are available, the following will be displayed:

NO ALTERNATE CYLINDER AVAILABLE

When marking or assigning alternate tracks, the following error messages may occur:

TRACK HAS ALREADY BEEN MARKED DEFECTIVE
TRACK HAS ALREADY BEEN MARKED ALTERNATE

Selected Read

For this test, the display will be:

READ DL0 (Y OR N)?

If the response is No, the next logical unit will be displayed. If the response is Yes, the current cylinder address is displayed and each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message. The ASSIGN ALTERNATE TRACK message appears, and error messages if the track has been marked DEFECTIVE or ALTERNATE.

Random Seek, Read

For this test, the display will be:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND HEADS)?

This test selects a random cylinder, logical unit, and a sector address within the cylinder. The test then reads data and tests for errors. All logical units are used in this test. Alternate cylinders cannot be assigned during this test. The terminal keyboard space (SP) character is used to exit this test.

If an error is detected, the register content and locations are displayed with the 4-line identification message.

This check also ensures controller mapping is correct.

Random Seek, Write Data, Read Data, Compare Test

If the response is No, each logical unit will appear in sequence until the response is Yes:

DL0?
DL1?
DL2?
DL3?

This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows logical units to be tested. The terminal keyboard space character (SP) is used to exit from this test.

This test ensures that the controller is executing the write check command correctly and ensures that the controller is zero-filling the disc correctly.

Test ECC Logic

The following message will appear for this test:

TEST ECC?

DL0:?
DL1:?
DL2:?
DL3:?

ARE YOU SURE?

If ECC testing is selected, answering "Y" to "TEST ECC?" the program will prompt the operator to specify a unit. The unit selected will then be used to test the ECC logic.

Note

The unit selected will be written on.

The program selects whether a correctable or noncorrectable error is to be programmed; then the program creates an error; writes the sector with the error to the disc; reads to memory; then the program decides whether the error is noncorrectable or correctable.

If noncorrectable, the program checks to ensure an error has been returned by the controller.

If correctable, the program checks to make sure there has been no error returned by the controller, and checks to ensure the error was corrected in the proper manner. If this test fails, the message is one or more of the following:

CONTROLLER INDICATES CORRECTABLE ERROR

CONTROLLER INDICATES NONCORRECTABLE ERROR

ERROR BURST IS CORRECTABLE

ERROR BURST IS NONCORRECTABLE

ERROR BURST WAS NOT CORRECTED

The space character (SP) is used to exit from this test.

Assign Alternate Track

This test may be used if the disc drive manufacturer provides a map describing defective tracks. The message is:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK (Y OR N)?

If the response is No, the program will revert to:

USE R TO REPEAT

USE O TO TRANSFER TO ODT

USE L TO REBOOT YOUR SYSTEM

If the response is Yes, the display will be:

PHYSICAL DRIVE (0 or 1)? (Only if two drives are present)

CYLINDER ADDRESS (0 TO ____)

Enter the cylinder address, in decimal, of the defective track. If the cylinder address entered is incorrect, the message will be repeated.

The next message will be:

HEAD ADDRESS (0 TO ____)

Enter the head address, in decimal, of the defective track. If the head address entered is incorrect, the message will be repeated.

The next message will be:

MAP OUT

CYLINDER _____ HEAD _____

ARE YOU SURE? (Y OR N)

If No, the program will repeat the first message of this test. If Yes, an alternate cylinder is assigned and the message is:

ALTERNATE CYLINDER ASSIGNED

Other messages to appear may be:

TRACK ALREADY MARKED DEFECTIVE

or

TRACK ALREADY MARKED ALTERNATE

The program will then repeat the first message of this test.

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function — The expected activity of the disc system (write, seek, read, etc.).

Command — To initiate a function (halt, clear, go, etc.)

Operations — One or more orders executed in a prescribed sequence that causes a function to be performed.

Address — The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register — An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system.

OPERATIONS

WRITE—When the controller is given a write command it will perform the mapping algorithm, do an implied seek if one is necessary, and then do the write operation. The controller will perform spiral operations until the word count is exhausted, unlike the real RL controller.

READ—The read is performed like the write, except for the direction of data flow.

RESTORE—The real RL controller does not have an implicit restore command, so the restore operation has been incorporated into the "Get Status" command. When a "Get Status" is performed, and bit 4 of the RLDA register is set, the selected disc drive will be positioned to track zero.

WRITE FORMAT—When a write command is issued to the controller and bit 15 of the RLMP register is a zero, the write data command will be changed to a write format command.

Format commands read/write a fixed buffer size of 51 words. The format commands start and end at the index signal from the disc. There are 3 words from the table for each of the 17 headers in a track. The physical position of a header in the table determines its physical position in the track.

When a read/write command is issued with bits 15 and 14 reset, the firmware responds to this as a format command with inhibit seek. The firmware will perform the desired format command on the head addressed by the RLDA in map override form, but will not do any seek previous to the command.

When read/write command is issued with bits 15 reset and bit 14 set, the firmware responds to this as a format command with seek and map override. The firmware will use the RLDA as real head and cylinder addresses, will seek to the desired position in the disc and perform the desired read/write format function.

The general flow of a program to format the disc is of a 4 pass operation. In pass one the headers are written, and the controller erases all the data fields. In pass two the headers are verified. In pass three the disc data fields are written and in pass four the data fields are verified.

The initial command in the formatting program is to do a restore on the physical unit. The restore command does not require any cylinder calculations, so it can be performed on an unformatted disc drive.

When the drive has been restored to track zero, then head zero can be written with a write format/inhibit seek. This command, since it also does no cylinder calculations can be performed on an unformatted disc drive.

Once cylinder zero, head zero has been formatted, then commands with seeks can be performed.

READ FORMAT—When a read command is issued to the controller and bit 15 of the RLMP is a zero, the read data command will be changed to a read format command.

SEEK—Since the physical characteristics of the disc do not match the RL01/RL02 it is emulating, the normal seek command is essentially worthless and does no operation on the real disc. All read/write commands are preceded with an implied seek operation that is performed by the firmware. Whenever the firmware is required to do an implied seek, it will verify its new disk position (format commands excepted). An implied seek will also occur when a command continues across a real disc cylinder boundary.

The implied seek operation consists of reading the first available header. The firmware then calculates the difference in real cylinders between its present position, and the desired position. The firmware then issues step pulses to the disc at timed intervals. When the heads have settled at the new cylinder, a header is read and the cylinder address is verified by firmware to be correct.

WRITE CHECK—The command begins like a read command, and finds the requested sector on the disc, and reads it into the controller's data buffer. The firmware will then DMA data from the

computer and compare the data against the data in the buffer. A miscompare will set the data error status.

CONTROLLER CLEAR—The command will clear the RLBA and RLAE and RLDA registers and the error status in the RLCS register. The RLMP most significant byte will be cleared, then bits 15 and 14 set (to avoid accidental format commands). The RLMP least significant byte will be loaded with the revision number of the microcode. This command duplicates the effects of a bus initialization, except the microcode does not do the self test.

WRITE DIAGNOSTIC MODE—The command is restricted to a one sector operation. It is also to be done only on the last physical sector in a track. The command is a write data command with bit 14 of the RLMP cleared. The word count is to be one sector plus 2 words. The RLMP value is then octal 137376. The command will write the data buffer and instead of appending the 32 bit controller generated ECC check character to the end of the buffer, it will write the last two words of the data buffer as the ECC characters.

READ DIAGNOSTIC MODE—The command is restricted to a one sector operation. There is no restriction on the disc address. The data buffer passed to memory will begin with the third word of the data field. The last two words of the data buffer will contain the ECC check character read from the disc. The data error status is indeterminate during this command, and should be ignored.

INTERRUPTS

The controller will interrupt after commands complete if bit 6 of the RLCS is set. Note that doing a BIS of bit 6 to the RLCS does not give an interrupt, as in some other controllers.

DIAGNOSTIC

The diagnostic is named DQ614, available from the software department. The revision of the diagnostic will be displayed on the startup message.

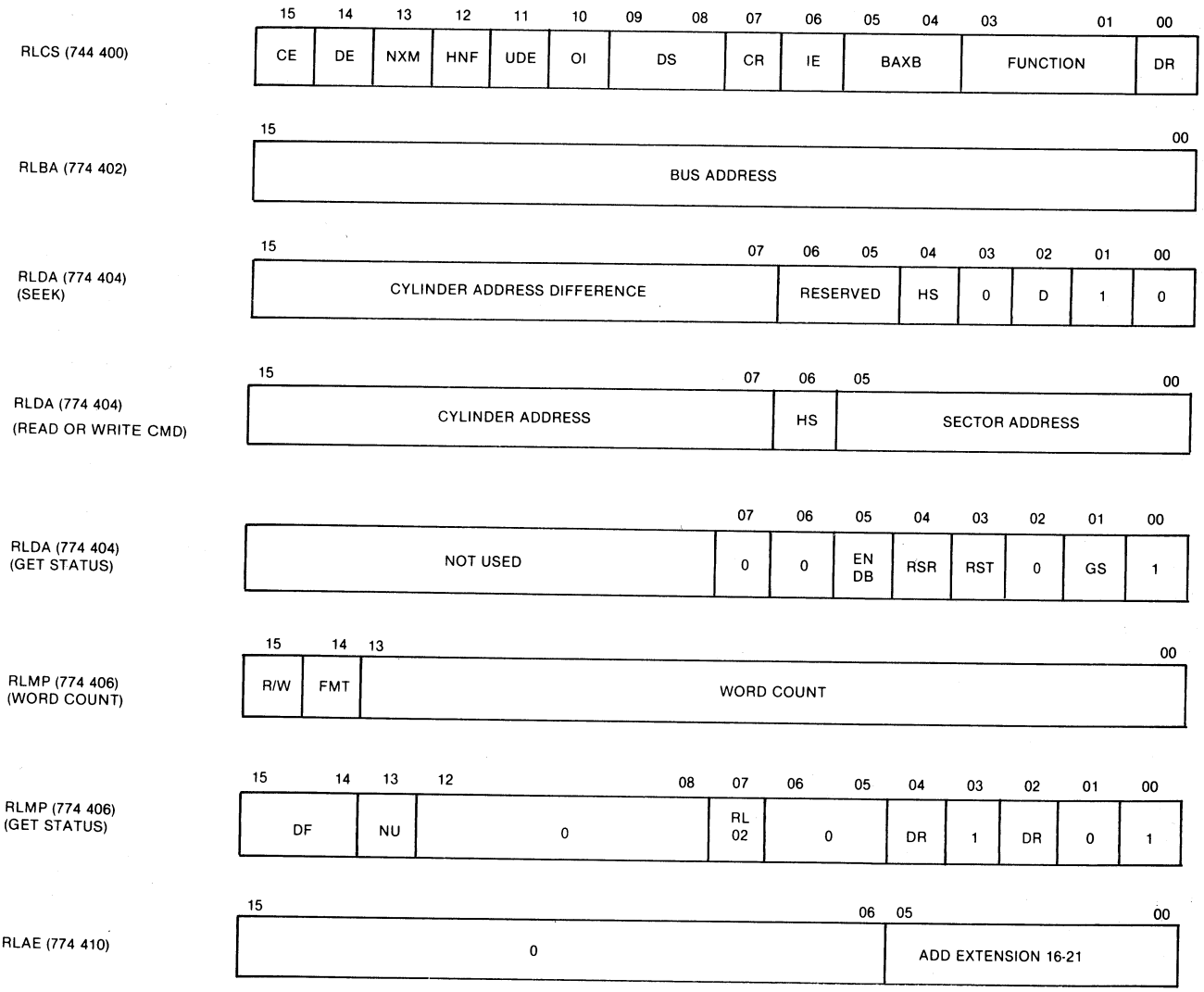
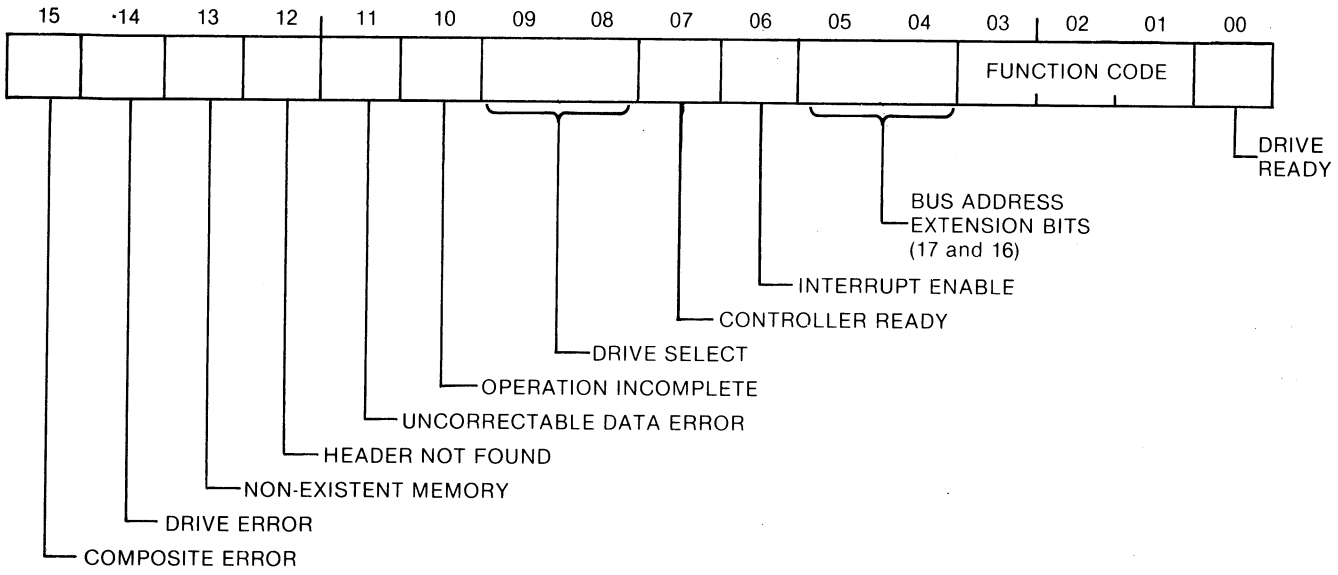


Figure 4-1. Register Summary

Control/Status Register
774 400 (RLCS)

The Control/Status Register (RLCS) has the bus address 774 400. The purpose of the register is to pass commands to the controller, and to pass status back to the program.

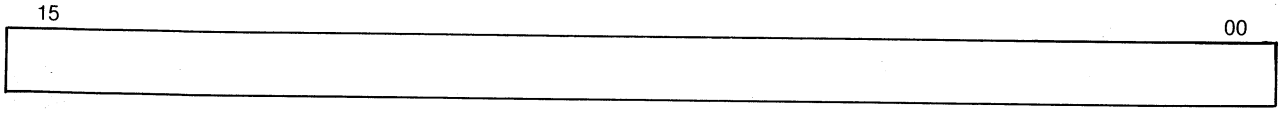


BIT(S)	DESCRIPTION
00	DRIVE READY—When set, indicates drive is ready.
01, 02, 03	FUNCTION CODE—The function code is a three bit field that defines one of eight possible commands to the controller.

COMMAND 0 (0 0 0)	Controller Reset—This command will reset the controller and the internal flags. At the completion of the command the revision number of the microcode will be in the LSB of the multipurpose register. This command is similar to the Bus Initialization signal except that the "INIT" signal also causes the microprocessor to perform its self test.
COMMAND 1 (0 0 1)	Write Check—This command will compare a table in memory against the data on the disc. A miscompare will set the uncorrectable error status. The controller will not perform error correction on the data read from the disc.
COMMAND 2 (0 1 0)	Get Status—This command is used to obtain the drive status, restore the disc, and Read/Write into the controller data buffer for diagnostic purposes. The exact operation is determined by bits in the RLDA Register.
COMMAND 3 (0 1 1)	Seek—This command will present status to the program to indicate a seek is performed, but no action will really take place. The controller functions with transparent seeking taking place after the mapping algorithm is performed, so this command is essentially a NO-OP.
COMMAND 4 (1 0 0)	Read Headers—This command will present status to the program to indicate a read headers is performed but no action will really take place. The software uses this command in conjunction with the seek command, which is also essentially a NO-OP as this one.
COMMAND 5 (1 0 1)	Write Data—This command will write data blocks onto the disc. Alternately if bit 15 of the multipurpose register is a zero, the command will write headers onto the disc, and erase the data fields (a write format command).

	COMMAND 6 (1 1 0)	Read Data—This command will read data blocks from the disc. Alternately if bit 15 of the multipurpose register is a zero, the command will read headers from the disc. (A read format command.)
	COMMAND 7 (1 1 1)	Read Data—This command will function as command six, but if command six encounters an uncorrectable data field it will stop, and not transfer bad data. This command will transfer the bad data before halting the operation.
04, 05		BUS ADDRESS EXTENSION BITS (17 and 16)—These bits are Bus Extension bits 17(5) and 16(6). These are identical to bits 1 and 0 of RLAE Register and can be set by writing into either register. These bits increment everytime the RLBA Register overflows.
06		INTERRUPT ENABLE—When set, this bit allows the controller to interrupt the processor at the end of an operation.
07		CONTROLLER ENABLE—When cleared by the software, this bit indicates that the controller is to start an operation. When set by the controller, this bit indicates that the controller is ready to accept another command.
08-09		DRIVE SELECT—These bits determine which of four logical units is selected.
10		OPERATION INCOMPLETE—The Operation Incomplete status when set, indicates that the controller passed the initial requirements to start the operation, but that an error was encountered during operations.
11		UNCORRECTABLE DATA ERROR—The ECC Error Status when set, indicates that the controller has made two attempts to read the data and has been unable to correct the error. Refer to Table 2-1 for the implications of Switch one on this status.
12		HEADER NOT FOUND—The Header Not Found status when set, indicates that the controller has searched the data track for three spins of the disc and has not been able to locate the desired data block.
13		NON-EXISTENT MEMORY—The Non-Existent Memory status when set, indicates that during a DMA cycle the controller as Bus Master, did not receive a response from the memory addressed within 20 μs.
14		DRIVE ERROR—The Drive Error bit when set, indicates the controller has determined that there exists a problem in the drive that will not allow the command to proceed further. This bit can be set if the controller determines that (1) The drive has gone "NOT READY", (2) The drive fault line goes true, (3) The drive selected status from the drive goes false during a command, (4) During any transparent seek operation if the controller detects a positioning error during its verify positioning cycle, (5) If the continuation of an operation will attempt to exceed the end of a logical unit.
15		COMPOSITE ERROR—The Composite Error bit when set, indicates that one or more of the error bits (14-10) is set.

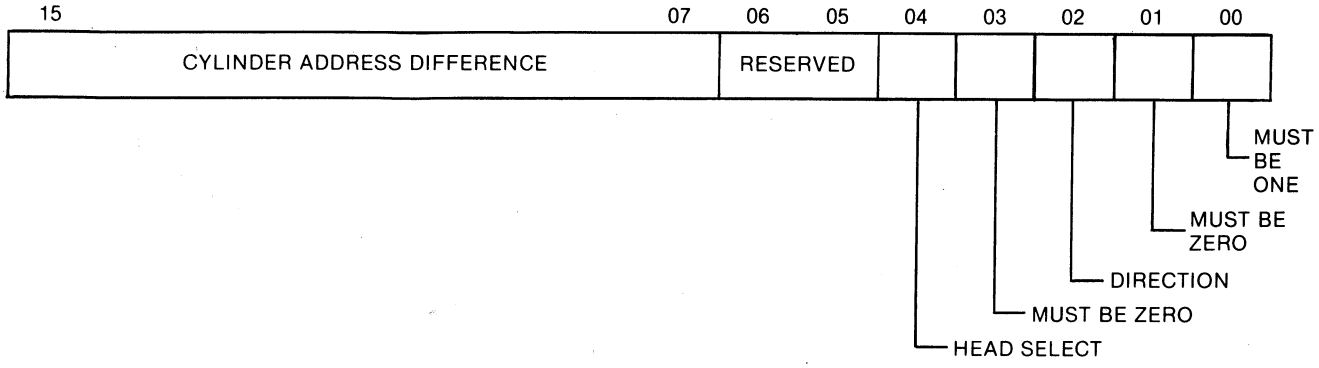
BUS ADDRESS REGISTER (RLBA) 774 402



The address of RLBA is 774 402. The bits of this register contain the bus address of data transferred during read or write check operations. The register is incremented by two at the end of each transfer. If the system has extended memory, the RLBA will overflow to the EX MEM bits (04, 05) of the RLCS to reflect the extended bus address. This is a read/write register cleared by INIT or RESET functions.

DISC ADDRESS REGISTER
774 404 (RLDA)

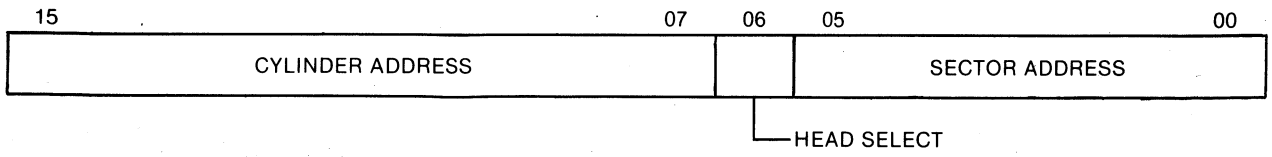
The Disc Address register has the bus address of 774 404. The purpose of the register is to pass disc addresses to the controller.



RLDA on a SEEK command.

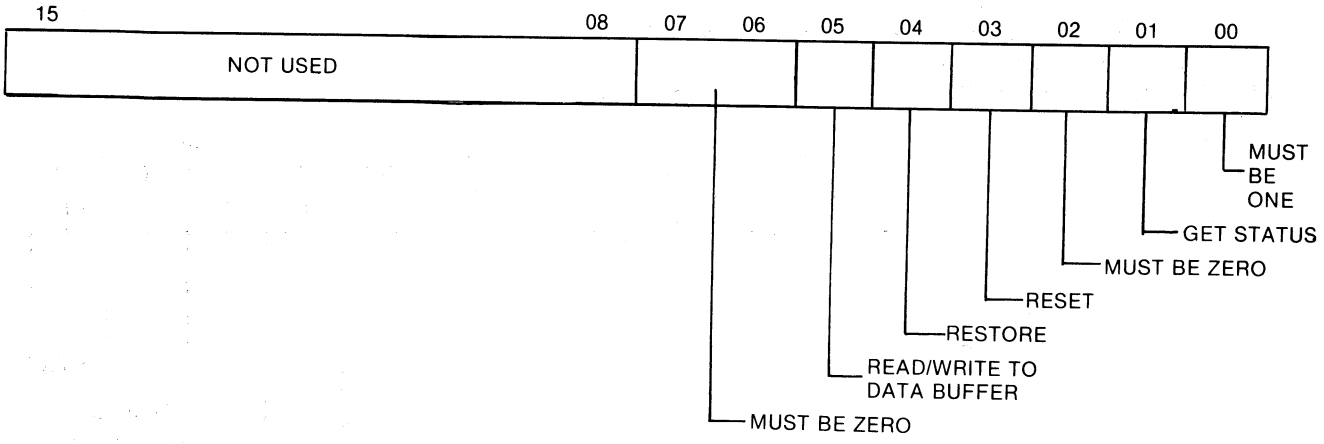
BIT(S)	DESCRIPTION
00	Must be 1
01	Must be 0
02	DIRECTION—This bit indicates the direction in which a seek is to take place. When the bit is set, the heads move to a higher cylinder address. When the bit is cleared, the heads move to a lower cylinder address.
03	Must be 0
04	HEAD SELECT—This bit indicates which head (disc surface) is to be selected. Set=lower, clear=upper.
05-06	Reserved
07-15	CYLINDER ADDRESS DIFFERENCE—These bits indicate the number of cylinders the heads are to move on a seek.

RLDA on a READ or WRITE data command.
(RL01/RL02 Disc Address)



BIT(S)	DESCRIPTION
00-05	SECTOR ADDRESS—These bits indicate the addressed sector.
06	HEAD SELECT—This bit indicates which head (disc surface) is to be selected. Set=lower, clear=upper.
07-15	CYLINDER ADDRESS—These bits indicate the address of the cylinder being accessed.

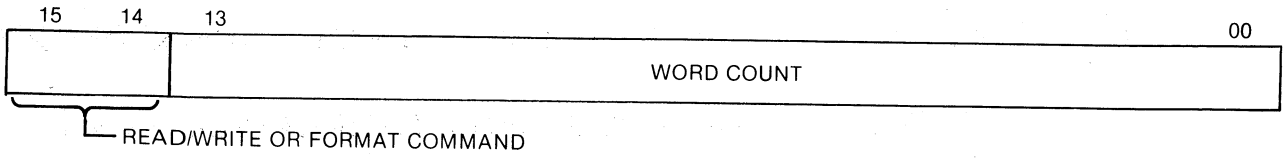
RLDA on a GET STATUS command.



BIT(S)	DESCRIPTION
00	Must be 1
01	GET STATUS—When set, enables status to be put into the Multipurpose Register by Get Status function code.
02	Must be 0
03	RESET—When set, causes the drive to clear its Error Register before sending a status word to the Controller.
04	RESTORE—When set, this bit causes the heads to return to cylinder 0.
05	READ/WRITE TO DATA BUFFER—When set on a get status command, allows access to the controller internal data buffer. When the programmer outputs a word to the Multipurpose Register it will be written into the internal data buffer. When the programmer inputs a word from the Multipurpose Register the word will be read from the internal data buffer.
06-07	Must be 0
08-15	Not Used

MULTIPURPOSE REGISTER 774 406 (RLMP)

The Multipurpose register has the bus address of 774 406. The purpose of the register is to pass the word count to the controller on a read/write command, and to pass disc status back to the program on a get status, and to move data into/out of the controller buffer during a diagnostic test.

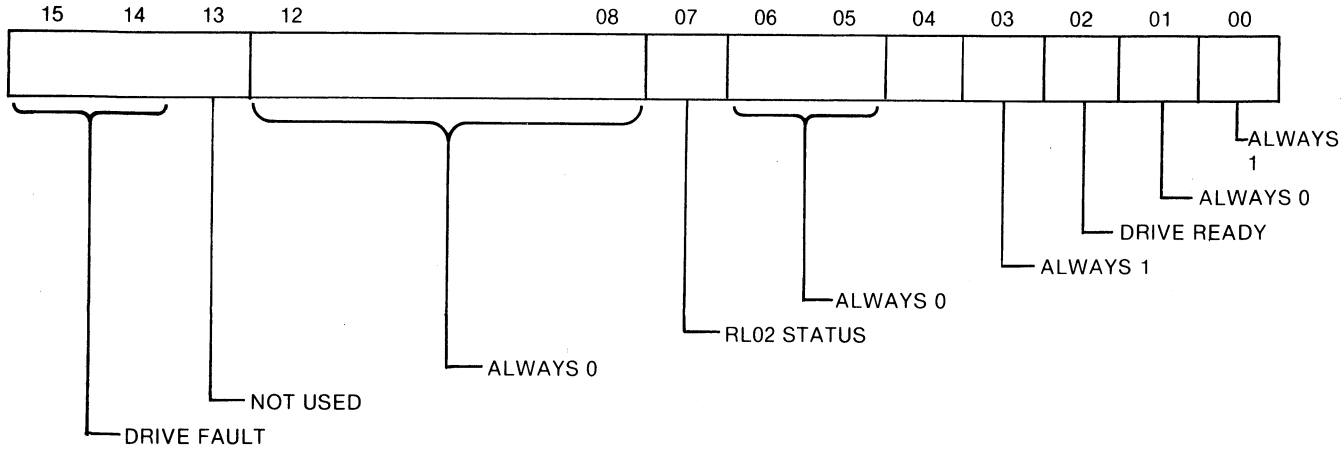


During Read/Write Command for Word Count

BIT(S)	DESCRIPTION
00-13	WORD COUNT—These bits are the 2's complement of the total number of words to be transferred during a read, write or write check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is completed and the controller action is terminated at the end of the current disc sector.
14-15	These bits indicate the following: 15, 14 SET; Read/write data command. 15 SET, 14 CLEAR; Read/write data command with ECC Diagnostic Mode. 15 CLEAR, 14 SET; Format command with seek. 15 CLEAR, 14 CLEAR; Format command with no seek.

During a Get Status Command

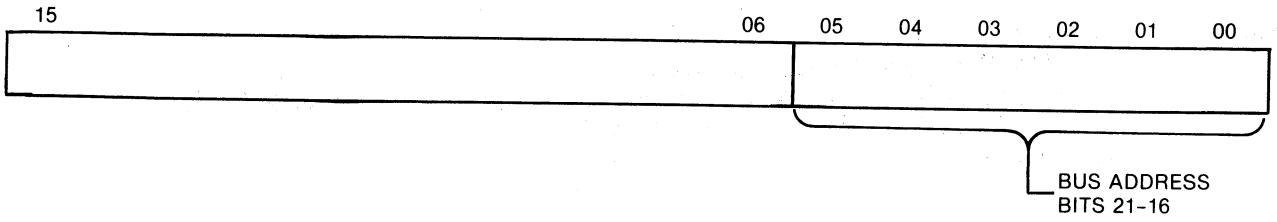
RLMP is used to read/write the data buffer by using the GET STATUS command with bit 5 or RLDA.



BIT(S)	DEFINITION
00	Always 1.
01	Always 0.
02, 04	DRIVE READY—When bits 02 and 04 are set, the drive is ready for operation.
05-06	Always 0.
07	RL02 STATUS—When set drive is RL02. When clear drive is RL01.
08-12	Always 0.
13	Not Used
14-15	DRIVE FAULT—Sets if an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.

ADDRESS EXTENSION REGISTER
774 410 (RLAE)

The Address Extension register has the bus address 774 410. The purpose of the register is to hold the extra memory address bits not held in the RLBA.



SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the disc drive manufacturers manual. Ensure power is off when connecting or disconnecting board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.

2. Verify that all switches are properly set as described in Sections 2 and 3.

3. Verify that all modules are properly seated in the computer and properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disc drive generate the proper responses when the system is powered up.

2. Verify that the computer panel switches are set correctly.

3. Verify that the console can be operated in the local mode. If not, the console may be defective.

4. Verify that the green diagnostic light on the controller is on.

CONTROLLER SYMPTOMS

Controller symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +12V source is shown on sheet 11 (AD2), and the +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers on the logic diagrams.

ADJUSTMENT PROCEDURE FOR DATA SEPARATOR

This procedure should be performed only when a component is changed in the phase-locked loop circuitry. A two-channel oscilloscope, a frequency counter, and an extender board are required for this adjustment.

CAUTION

This adjustment is factory set and the components sealed with glyptol. The adjustment should be performed in field by a qualified technician only.

Component locations are shown on Figure 2-1. Proceed as follows:

1. Place the controller on an extender board.

2. Power up the computer and run it to warm-up the controller to operating temperature.

Note

Do not connect the drive for this adjustment.

Table 5-1. Controller Symptoms

Symptom	Possible Causes	Check/Corrective Action
1. Green DIAG light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator (Sheet 11,U12,Y1) b. Short or open on board c. Bad IC d. PROMs not properly seated (U13 through U8)	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901 (Sheet 6). All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitute pulses. Check +12V (Sheet 11) and +5V at various IC's. Check PROM's 1 through 7 for proper seating. Check oscillator Y1.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. DEN always low (Sheet 3) b. Shorted bus tranceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal DEN for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches. Check cable connections. Controller Registers/Using ODT, examine controller register RLCS, bit 0 and 8 and 9. These bits represent DISC UNIT READY AND SELECTED and must be present for proper communication. Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from disc incorrect	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Test and Format Program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specefied in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure—Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad component.

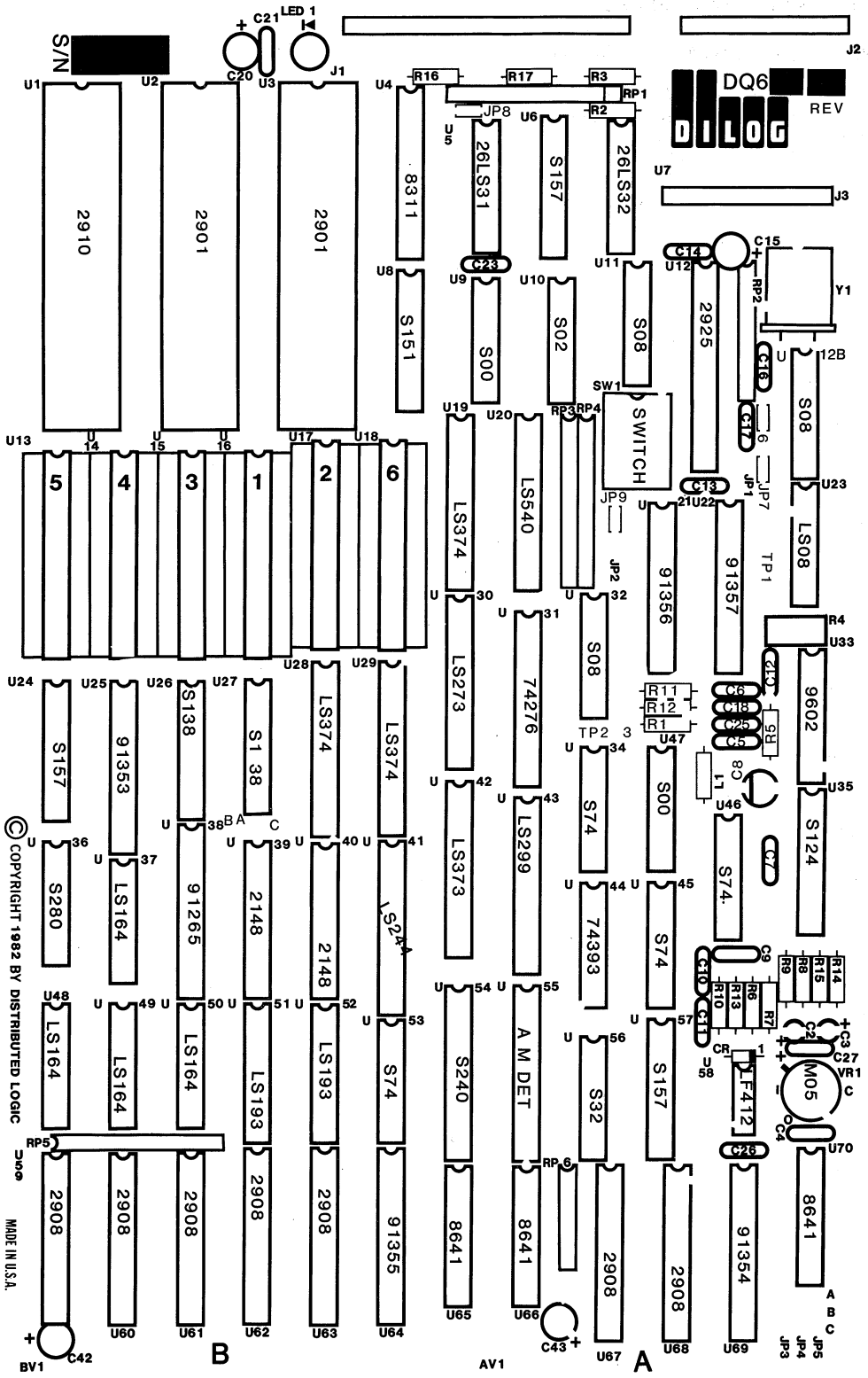


Figure 5-1. Board Layout

Table 5-2. Term Listing

Term	Source	Destination	Description
AMSRCH+	10	8, 11	Address Mark Search
BBS7	BUS (AP2)	1	Bus Peripheral Address Select
BBS7+	1	3	Peripheral Address Select
BDIN	BUS (AH2)	1	Bus Data In
BDIN+	1	3, 9	Data In
BDA00	BUS (AU2)	2	Bus D/R0
BDA01	BUS (AV2)	2	Bus D/R1
BDA02	BUS (BE2)	2	Bus D/R2
BDA03	BUS (BF2)	2	Bus D/R3
BDA04	BUS (BH2)	2	Bus D/R4
BDA05	BUS (BJ2)	2	Bus D/R5
BDA06	BUS (BK2)	2	Bus D/R6
BDA07	BUS (BL2)	2	Bus D/R7
BDA08	BUS (BM2)	2	Bus D/R8
BDA09	BUS (BN2)	2	Bus D/R9
BDA10	BUS (BP2)	2	Bus D/R10
BDA11	BUS (BR2)	2	Bus D/R11
BDA12	BUS (BS2)	2	Bus D/R12
BDA13	BUS (BT2)	2	Bus D/R13
BDA14	BUS (BU2)	2	Bus D/R14
BDA15	BUS (BV2)	2	Bus D/R15
BDA16	BUS (AC1)	1	Bus Extension Bit 16
BDA17	BUS (AD1)	1	Bus Extension Bit 17
BDAL18	BUS (BC1)	3	Address Extension Bit 18
BDAL19	BUS (BD1)	3	Address Extension Bit 19
BDAL20	BUS (BE1)	3	Address Extension Bit 20
BDAL21	BUS (BF1)	3	Address Extension Bit 21
BDMGI	BUS (AR2)	1	Bus DMA Grant In
BDMGO	BUS (AS2)	1	Bus DMA Grant Out
BDMR	BUS (AN1)	1	Q Bus Request
BDOUT	BUS (AE2)	1	Bus Data Out
BDOUT+	1	9	Data Out
BFULE+	10	8	Enable Buffer Ful
BIAKI	BUS (AM2)	1	Bus Interrupt Acknowledge In
BIAKO	BUS (AN2)	1	Bus Interrupt Acknowledge Output
BINIT	BUS (AT2)	1	Initialize—Clear Devices on I/O Bus
BIRQ4	BUS (AL2)	3	Host Interrupt Request 4

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
BIRQ5	BUS (AA1)	3	Host Interrupt Request 5
BIRQ6	BUS (AB1)	3	Host Interrupt Request 6
BIRQ7	BUS (BP1)		Host Interrupt Request 7
BIT+	8	12	9th Serial Data Path Bit
BIT4+	8	13	Half Byte Flag for ECC
BPOK	BUS (BB1)	10	Primary Power OK
BRPLY	BUS (AF2)	1	Q Bus Reply
BSACK	BUS (DN1)	1	DMA Request Acknowledge
BSYNC	BUS (AJ2)	1	Synchronize I/O Address
BWTBT	BUS (AK2)	1	Control Write Byte
BYT8+	7	8	End Postamble Byte
BYT16+	7	8	End Data Time Byte
CI+	5	6	Carry In
CP0	7	2	Control Pulse 0
CP2–	7	5	Control Pulse 2
CP3–	7	10	Control Pulse 3
CP4–	7	9	Control Pulse 4
CP5–	7	10	Control Pulse 5
CP6–	7	8, 12	Control Pulse 6
COUT+	6	5	Carry Out
CORRV+	11	10	Voltage Correction for VCO
CR1-0/ CR1-2	4	5, 6	Microcode Instruction
CR1-3	3	6	Microcode Instruction
CR1-4/ CR1-6	4	6, 9	Microcode Instruction
CR1-7	4	6	Microcode Instruction
CR2-0/ CR2-1	4	5	Microcode Instruction
CR2-2/ CR2-7	4	6	Microcode Instruction
CR3-1/ CR3-4	4	9	Microcode Instruction
CR3-0	4	5	Microcode Instruction
CR3-5/ CR3-7	4	6	Microcode Instruction
CR4-0	4	10, 5	Microcode Instruction
CR4-1	4	1, 5, 7	Microcode Instruction
CR4-2/ CR4-4	4	3, 5	Microcode Instruction
CR4-5/ CR4-7	4	5	Microcode Instruction
CR5-0/ CR5-3	4	1, 5, 7	Microcode Instruction
CR5-4/ CR5-7	4	5, 7	Microcode Instruction
CSA0+ CSA9+	5	4	Control Store Memory Address
CSTART–	3	11	Clock Start
CTCHME+	8	11	Parking Oscillator or Read Data
DATAIN+	12	8	Serial Data to Shift Register
DAT0+/ DAT7+	7	8	Data Buffer Data Bus
DEN–	3	2	Enable Data
DEN+	10	3	Enable Data
DIR	10	J1, 34	Direction of Seek
DMGI+	1	3	DMA Grant In
D0+/D1+	2	4, 6, 7, 9	D Bus Bits 0-1

Table 5-1. Term Listing (Continued)

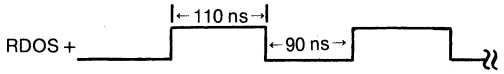
Term	Source	Destination	Description
D0+/D1+	1	2, 4, 6, 7, 9	D Bus Bits 0-1
D2+/D7+	2	3, 4, 6, 7, 9	D Bus Bits 2-7
D6+/D7+	1	2, 4, 6, 7, 9	D Bus Bits 6-7
DRSL0	10	J1, 26	Select Drive 0
DRSL1	10	J1, 28	Select Drive 1
DRVSL1−	J3, 1	10	Drive 1 Selected
DRVSL0	J2, 1	10	Drive 0 Selected
EADD−	3	1	Enable Address Q Bus Control
ECCEN+	13	12	ECC Enable
ECCERR+	13	8, 12	ECC Error
ECCTIM−	13	8, 12	ECC Byte Time-End Block
ENDC+	7	8	End Count
EMUX−	8	13	End of Header or Data
EPCOMP+	10	13	Enable Precompensation of Write
FAULT	J1, 12	10	Drive Fault
GSCLK−	11	5	System Clock
HESL1	10	J1, 14	Head 1 Select
HESL2	10	J1, 18	Head 2 Select
HESL3	10	J1, 4	Head 3 Select
IAKI+	1	3	Host Interrupt Acknowledge In
IAKIG−	3	9	Interrupt Acknowledge
INDEX	9	J1, 20	Disc Index Mark
INIT+	1	3	Initialize
LXR0−	9	2	Destination Decode-Transceiver Clock
LXR1−	9	2	Destination Decode-Transceiver Clock
LXR2−	9	7	Destination Decode-Load Address Register
LXR3−	9	8	Destination Decode-Load Y Register
LXR4−	9	10	Destination Decode-System Control Register
LXR5−	9	10	Destination Decode-Drive Control
LXR6−	9	1, 3	Destination Decode-Transceiver and Extension Clock
LY+	8	7	Load Y
MFI0+	3	5	Manufactured Instruction Bit 0 for 2910
NEWBYT+	8	13	New Byte to Shift Register
QCLK−	3	1, 7	Clock
RAMEN−	8	7	Enable Buffer
RDAT0	10	J2, 18	Read Data Drive 0
RDAT0+	10	J2, 17	Read Data Drive 0
RDAT1−	10	JJ, 18	Read Data Drive 1
RDAT1+	10	J3, 17	Read Data Drive 1
RDOS+	11	8	Read Data One Shot
READY−	10	9	Ready
REDUCI	10	J1, 2	Reduce Write Current
RESET−	3	1, 4, 5, 10	Controller Reset
RMFM	10	8	Read Modified Frequency Modulation
ROMCLK−	11	4, 8, 13	200NS Clock
RPLY+	1	3, 9	Reply From Slave
RSYNC+	1	2, 9	Synchronize 2901 to Host I/O Lines
SCLK−	11	3, 6, 9	150NS Hi, 50NS Lo
SEEK COMPLETE	9	J1, 8	Disc Seek Complete
SLIN+	3	5	Slave Interrupt Acknowledge Request
SREN+	13	8	Shift Register Enable

Table 5-2. Term Listing (Continued)

Term	Source	Destination	Description
STEP	10	J1, 24	Step Pulse to Disc
STOP−	8	9, 10	Read or Write Operation Complete
TIAKO	3	1	Interrupt Acknowledge
TDMG+	3	1	Bus Grant to D/R
TDMR+	10	1, 3	Transmit Direct Memory Grant
TIRQ+	10		Interrupt Request
TRACK ZERO	9	J1, 10	Disc Track Zero
TSACK−	3	1, 9	System Acknowledge
UNCLAMP+	10	11	Reset PLL
UNLOCK+	10	9	Voltage Correction for VCO Status
VCO+	11	8	Voltage Controlled Oscillator
VEC+	5	4	Vector Address Register Out
WDATA+	12	13	Write Data
WDAT0−	18	J2, 14	Write Data Drive 0
WDAT0+	10	J2, 13	Write Data Drive 0
WDAT1−	10	J3, 14	Write Data Drive 1
WDAT1+	10	J3, 13	Write Data Drive 1
WOS+	9	10	Write One Shot
WPLS−	13	9	Write Pulse
WPROT0	1	J2, 5	Write Protect Unit 0
WPROT1	1	J3, 5	Write Protect Unit 1
WGT+	10	9, 13	Write Gate
WRAM−	8	7	Write to RAM
WREN+	10	8	Write Enable
WRITE GATE	10	J1, 6	Write Gate
XSD0−/ XSD1−	9	2	Enable Transceivers
XSD3−	9	7	Enable Bus Driver
XSD5−	9	1, 3	Enable Transceivers-Extension Bits
XSD6−	9	7	Enable Boot PROM Switched
XSD7−	9	7	Enable Boot PROM Ungated
YD−	8	7	Enable Buffer Address Register
Y0+/Y1+	6	1, 2, 5, 7, 10	Y Bus
Y2+/Y3+	6	2, 3, 5, 7, 10	Y Bus
Y4+/Y5+	6	2, 3, 5, 7, 10	Y Bus
Y6+	6	1, 2, 5, 7, 10	Y Bus
Y7+	6	2, 5, 7, 10	Y Bus
ZERO+	6	5	2901 Output at Zero
1+	11	8	50NS Pulse (phase 1)
10 MHZ+	11	3, 13	10 MHZ Clock

3. Connect channel A to TP1 (RDOS+).

4. Adjust R4 (channel A) for 110 nanoseconds high and 90 nanoseconds low as shown:



5. Connect the frequency counter to TP2 (VCO−).

6. Observe 10.0 MHz on the frequency counter. This is the value at which VCO− locks.

7. Jumper TP3 (VCLAMP+) to ground.

8. The frequency counter should be at 8.5 MHz. If required, adjust C8 to 8.5 MHz +0.25, −0 MHz.

9. Remove ground from TP3.

10. Connect channel B to U58, pin 1 (CORRV+).

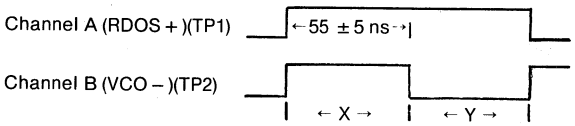
11. Observe the voltage and note for later reference (step 17). The voltage should be 3.0 ±0.2V and the VCO locked at 10 MHz.

12. If these values are not present, repeat step 7 through 11 to speed up or slow down the VCO to obtain the proper voltage.

13. Disconnect the frequency counter.

14. Connect channel B to TP2.

15. The following relationship between channel A and channel B must occur.



As shown, the leading edge of the pulse on channel A should be 55 ±5 nanoseconds from the trailing edge of the channel B pulse so that the X-Y transition of channel B is approximately centered with the channel A pulse.

16. If there is jitter on channel B, R4 should be readjusted to eliminate jitter.

17. Carefully seal the components with glyptol to avoid changing the settings. Before the glyptol sets check U58, pin 1 (voltage noted in step 11). If out of adjustment, quickly readjust C8 before the glyptol sets.

18. Disconnect the oscilloscope and counter, remove the extender board, and seat the board in proper slot.

19. Refer to the procedures in Section 3 for operation.

THEORY

The controller may be examined as five functions: computer interface, microprocessor, data buffer, peripheral interface-write, and peripheral interface-read. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the disc drive are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and some of the functional components. Single lines in the illustration represent serial data and the wider lines represent parallel data. Clock timing is illustrated at the end of this section, and the circuit is shown on Sheet 11.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q-Bus of the LSI-11 computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the LSI-11 DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and used for "bus arbitration." Bus synchronization is fully controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disc controller is busy with internal functions and controller/disc data transfers.

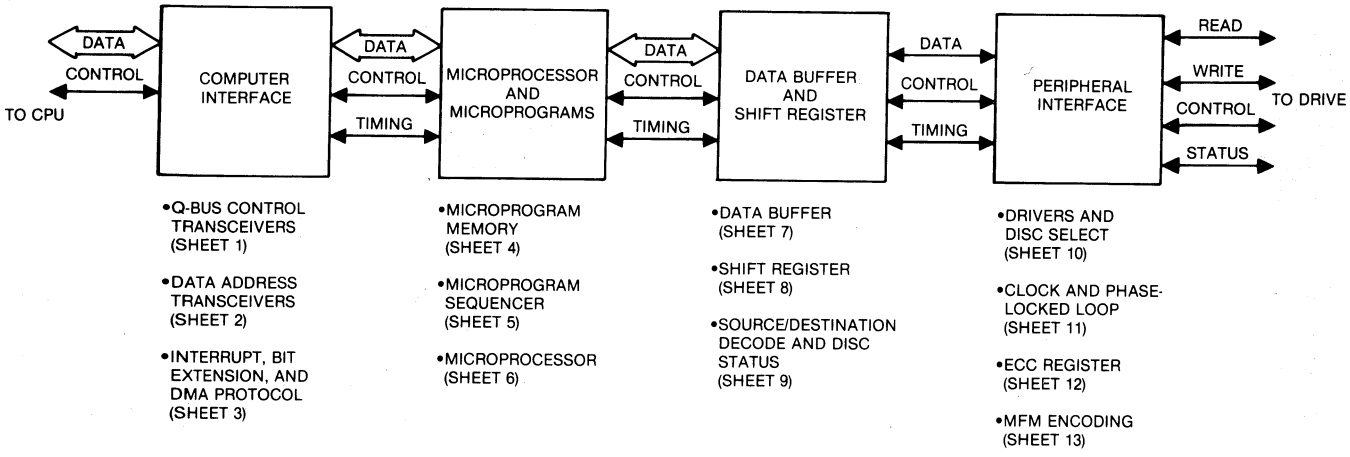


Figure 5-2. Simplified Block Diagram

All bus signals in this section are described in Table 1-1 or in the term listing. Control transceiver signals for the Q bus are shown on Sheet 1, components U65 through U68. Data and address transceiver are shown on Sheet 2. The bus control signals are designated BD and bus address and data signals are designated BDA. The latter are distributed as DBUS signals D0-D7.

On Sheet 3 there are two components designated PAL003 and PAL005. These components are called programmable arrayed logics. The PAL's can function as eight OR gates with eight AND gates of 32 inputs each with inverters, all of which are programmable. The outputs, F1 through F4 in U69 and F1 through F6 in U64, function as the outputs of flip flops.

The Interrupt Protocol, PAL003 on Sheet 3 is defined by components U69, U70, flip flop U34 and gate U12B. Bus Interrupt and Controller Interrupt Request lines, BIRQ4-7 and JP3-5, respectively, from U70, are input to the PAL for interrupt priority determination.

The signal BDIN (Data In) starts the Interrupt Acknowledge Sequence in U69. The output flip flop F2 samples the states of the bus and controller interrupt request lines. F2 will set if the controller is requesting an interrupt and there is no higher level interrupting device. When IAKI (Host Interrupt Acknowledge In) is received from the CPU, the state of F2 will determine if F3 is set (indicating the controller has the priority) or if F4 is reset (indicating the controller has lost the priority).

Bus transceiver U63 is for bits 18 through 21 of the 22-bit extension. These bits are held in the bus extension register, address 774 410.

PAL005 is the DMA Protocol and Sequence control. Flip flops F1 and F2 synchronize the DMA grant signal and determine if the controller is involved in the DMA queue. If the controller is requesting a DMA cycle, F3 will set notifying the microprocessor that it is the bus master. If the controller is not in the queue, F4 will reset which will pass the acknowledge to a lower priority.

Flip flops F5 and F6 monitor the bus controls and will handle the address/data multiplexing involved when the microprocessor is the bus master.

The output MFIO+ monitors the 3-bit field that is assigned to the microcode sequencer (U1, Sheet 5) and constructs the fourth bit that the sequencer requires.

Microprocessor Functions

The microprocessor (Sheet 6) is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read-only memory (PROM). The instructions, called "firmware," cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the LSI-11.

Because the disc and computer transfer data at different rates, it is necessary to buffer data going to and from the disc. High-speed RAM allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disc protocol are under microprocessor control. This feature allows modification of controller operating characteristics by making only changes to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the "Y Bus." Y Bus data governs all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destination decode IC's.

The "D Bus" is the data input of the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/destination decode logic on Sheet 9.

The following list describes D Bus enabling signals:

Function	Term	Component Enabled	Sheet
Data Transceivers MSB	XSD0-	U59, U60	2
Data Transceivers LSB	XSD1-	U61, U62	2
Q Bus Status	XSD2-	U29	9
Data Buffer	XSD3-	U39, U40	7
Disc Drive Status	XSD4-	U28	9
Q Bus Control/Extension	XSD5-	U68	1, 3
Bootstrap Enable	XSD6-	U12, U38	7
Constant Enable	XSD7-	U12, U38	7

All data on the D Bus is under control of the firmware as decoded by U27 on Sheet 9. The microprocessor selects the proper input data by enabling one of the above lines.

The Y Bus is the microprocessor output. Output of the microcode PROMs (Sheet 4) is decoded by U26 (Sheet 9) to select the destination of the data on the Y bus.

The following list describes Y Bus enabling signals.

Function	Term	Component Enabled	Sheet
Transceiver Driver Clock MSB	LXR0-	U59, U60	2
Transceiver Driver Clock LSB	LXR1-	U61, U62,	2
Buffer Address Register and Byte Counter	LXR2-	U44, U51, U52	7
RAM Write Control	LXR3-	U34, U54	8
System Control Register	LXR4-	U30	10
Drive Control/Head Select	LXR5-	U4	10
Q Bus Control/Extension	XLR6-	U68	1, 3

The microprogram sequencer, shown on Sheet 5, advances the program counter to the next address unless the condition code signal is active (output Z from PAL001). When CC is active, the jump address from the microcode is input to the sequencer.

Internal flip flops in PAL001 update the current microprocessor status. When signal CR3-0 is high, the flip flops retain the last microprocessor status. Bits CR4-5, -6, and -7 determine the condition code to test on conditional jump instructions to the sequencer. These signals are:

Bit 7	Bit 6	Bit 5	Description
0	0	0	Carry latch false
0	0	1	ALU equal to zero
0	1	0	Carry latch true
0	1	1	ALU not zero
1	0	0	Bit latch true
1	0	1	Slave latch true
1	1	0	Bit latch false
1	1	1	Unconditioned jump

The carry input (CI) signal to the microprocessor is determined by CR2-:

Bit 1	Bit 0	Description
0	0	No carry input
0	1	Bit test flop input
1	0	Carry latch input
1	1	Force carry input

RAM Data Buffer

The RAM data buffer is shown on Sheet 7. Data transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during a read or write operation. Once loaded, the contents of the buffer are then transferred to disc or memory in a completely separate operation.

During a write operation, address and parallel data (Y00-Y07) are transferred from memory via the microprocessor to the storage latch U42 and the data buffer address register, U51 and U52. The data is then transferred to the buffer and output (DAT0-DAT7) to the shift register.

During a read operation, parallel data is transferred from the shift register and input (DAT0-DAT7) to the data buffer. Timing for RAM address and chip select is shown in Figure 5-3.

Peripheral Interface-Write Data Path

A simplified diagram of the write path is shown in Figure 5-4. Parallel inputs (DAT0-DAT7) from the buffer are transferred to the shift register U43, Sheet 8. The output from QH is serial data which is selected by the read/write multiplexer, U57. The output Y0 is transmitted to flip flop U45, which creates a ninth bit, or holding bit, for the ECC register to permit ECC timing to catch up with the rest of the logic. The output signal from the flip flop is BIT+.

The outputs F1, F2, F3, F4, and F5 of PAL002 are described under "Read Data Paths." The resulting output of F6 PAL002 is the enabling signal for the data buffer to write. The signal F7 (NEWBYT+) is used on a write operation to flag the byte boundary for the shift register and the read/write sequencer (PAL006, Sheet 13). The signal F8 (STOP−) indicates to the microcode that a read/write operation is complete. The term WRAM- from gate U32 determines whether the logic writes to the buffer during a read operation or reads from the buffer during a write operation. The timing is shown in Figure 5-5.

ECC − Write

The ECC (error correction code) logic is shown on Sheet 12. The timing for ECC is shown in Figure 5-6. During a write operation, data (BIT+), is input to multiplexer U24 and to parity generator U36. The calculated check sum from U36 is input to the multiplexer at ECC time; the signal ECCTIM− goes low when the multiplexer shifts from the data path to ECC characters at the end of a field. The components U37, U48, U49, and U50 are parallel-out shift registers which generate the 32-bit polynomial, or check character. Switch 1 and flip flop U53 are used during a read operation and are described below. The output during a write operation is WDATA+ which is input to the write sequencer.

MFM − Write

The logic for the write sequencer and MFM encoding is shown on Sheet 13. The MFM (modified frequency modulation) encoding circuit basically accepts NRZI data, adds clocks, and rearranges the single output pulse stream to contain data and clock pulses. The circuit also compensates for the magnetic flux density phenomenon of peak shift; in high density packing, the pulses have a tendency to separate themselves at the point where a high frequency pulse stream meets a lower frequency pulse stream.

The pulse stream (WDATA+) from the ECC circuit is input to the write sequencer, PAL006, and to MFM encoding, PAL004. The single output stream of pulses is represented by WPLS−. The timing is shown in Figure 5-7 where "0" represents a clock pulse and "1" represents a data pulse on the WPLS− stream. (To simplify the diagram, EPCOMP (enable precompensation) and KILL (omit one pulse) are ignored at this time. The conditions for arranging the pulses are as follows:

1. If the WMFM cell is to hold a "0" (clock), a pulse will occur at the beginning of a cell.
2. If the WMFM cell is to hold a "1" (data, a pulse will occur at the center of a cell.
3. Pulses at the beginning of a cell are suppressed if the previous cell contains a "1".
4. There is never more than one pulse, either clock or data, in any bit cell.

The above conditions for placing a pulse on the stream are shown on the timing diagram. The output at F1, PAL006, is determined by ROMCLK−

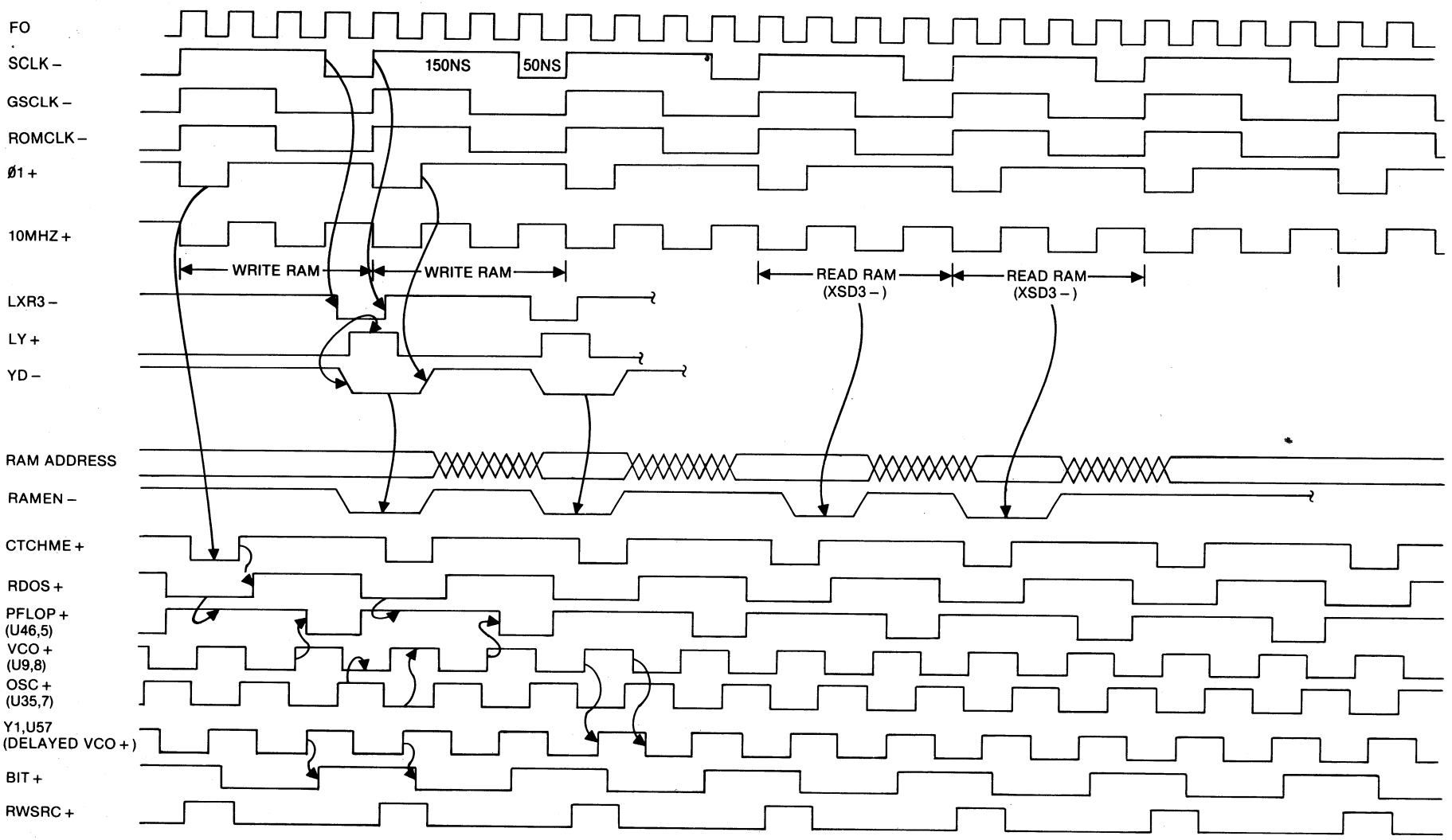


Figure 5-3. Ram Address Chip Select Timing

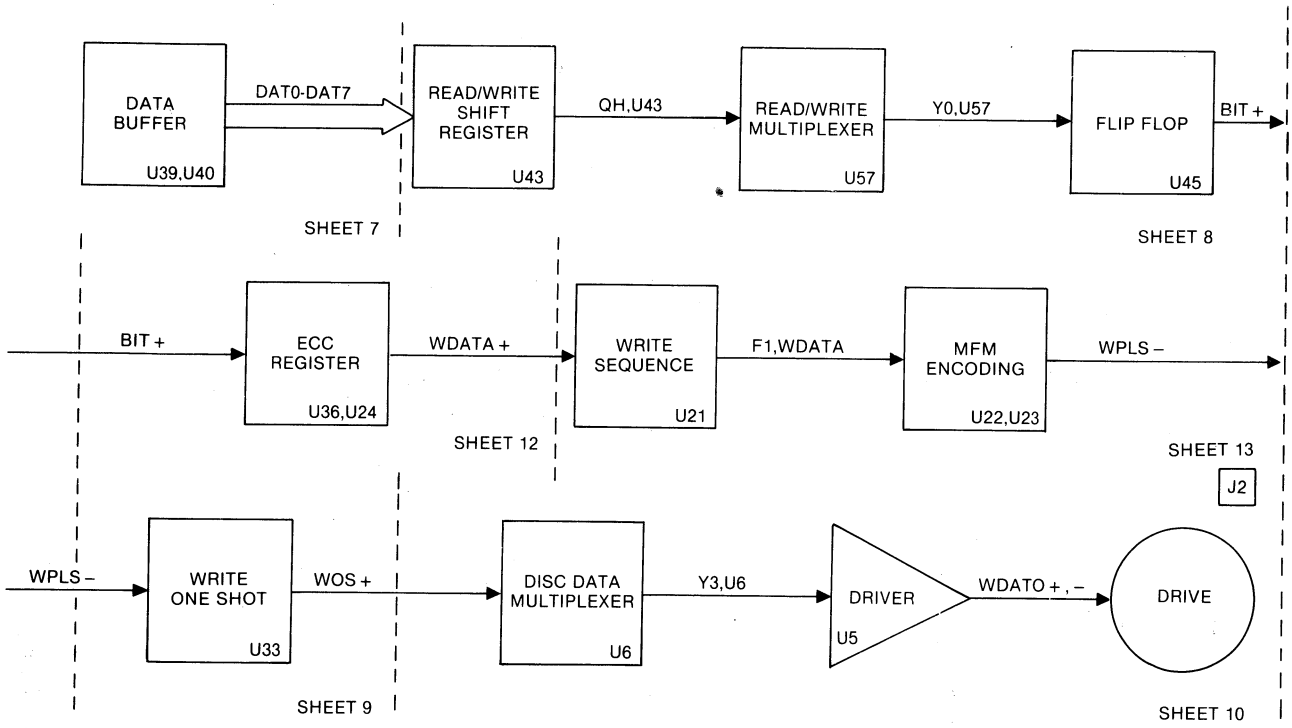


Figure 5-4. Write Data Path

and WDATA+. The equation for this relationship is F1=ROMCLK · WDATA + /ROMCLK · F1. The pulse stream may be further modified to compensate for peak shift. This phenomenon is illustrated in Figure 5-8. The outputs F1, F2, and F3 of PAL004 produce the MFM pulses: F1 produces the late pulse, 20 nanoseconds delay; F2 produces the center pulse, 10 nanoseconds delay; and F3 produces the early pulse, no delay. The center pulse is illustrated on the timing diagram by F2, PAL004. Table 5-3 lists the conditions for precompensation. F4 and F5 are internal flip flops in PAL004. The signal WDATA is input at C PAL004, and DATA is from F1 PAL006 to input A PAL004.

Table 5-3. Enable Precompensation

TERM						OUTPUT		
F5	F4	DATA	WDATA	ENABLE	PULSE	F1	F2	F3
X	X	1	X	EPCOMP	DATA CENTER		C	
X	0	1	0	EPCOMP	DATA CENTER		C	
X	0	1	1	EPCOMP	DATA LATE	L		
X	1	1	0	EPCOMP	DATA EARLY			E
X	1	1	1	EPCOMP	DATA CENTER		C	
X	0	0	X	EPCOMP	CLOCK CENTER		C	
0	0	0	0	EPCOMP	CLOCK CENTER		C	
0	0	0	0	EPCOMP	CLOCK EARLY			E
1	0	0	0	EPCOMP	CLOCK LATE	L		
1	0	0	1	EPCOMP	CLOCK CENTER		C	

X = Irrelevant

The signal EPCOMP (enable precompensation) on the table is false from cylinder zero until the disc reaches the cylinder identified during formatting, "Start Precompensation at Cylinder ____." This value is taken from the disc manufacturer's specification. The pulse column identifies data or clock and center, early or late. The output column identifies the flip flop outputs of PAL004 and whether the pulse is centered, early, or late.

Other outputs from PAL006 are as follows: F2 controls the enabling of the ECC register so that preamble information does not corrupt the polynomial. F3 delays the NEWBYT signal during writing to get the ECC timing into the time domain of the BIT+ flip flop (Sheet 8). F4 prepares for ECC time during a read operation and will enable the read ECC sync flip flop, U46, Sheet 13. F5 disables the write shift register (Sheet 8) during write format until the RAM enters a new header partition. F6 latches the output of the KILL flip flop (F8, PAL004) and remembers that the address mark is already written so that all succeeding X 'A1' characters do not get their clocks stripped. F7 is used in conjunction with F5 to hold the write shift register reset. F8 is used to signal that the ECC character time has arrived during a write command.

The output of F8, PAL004 (KILL) is used to create a unique pulse pattern for the address mark by "stripping" or omitting one clock pulse from the WPLS stream. The timing is illustrated in Figure 5-9.

From MFM encoding the pulse stream is input to the write one shot (U33, Sheet 9) where each pulse is shaped ("stretched") into a 70 nanosecond pulse for transmittal to the drive. The stream is then multiplexed to write data by U6, Sheet 10, and driven by the driver U5 as WDAT0 or WDAT1.

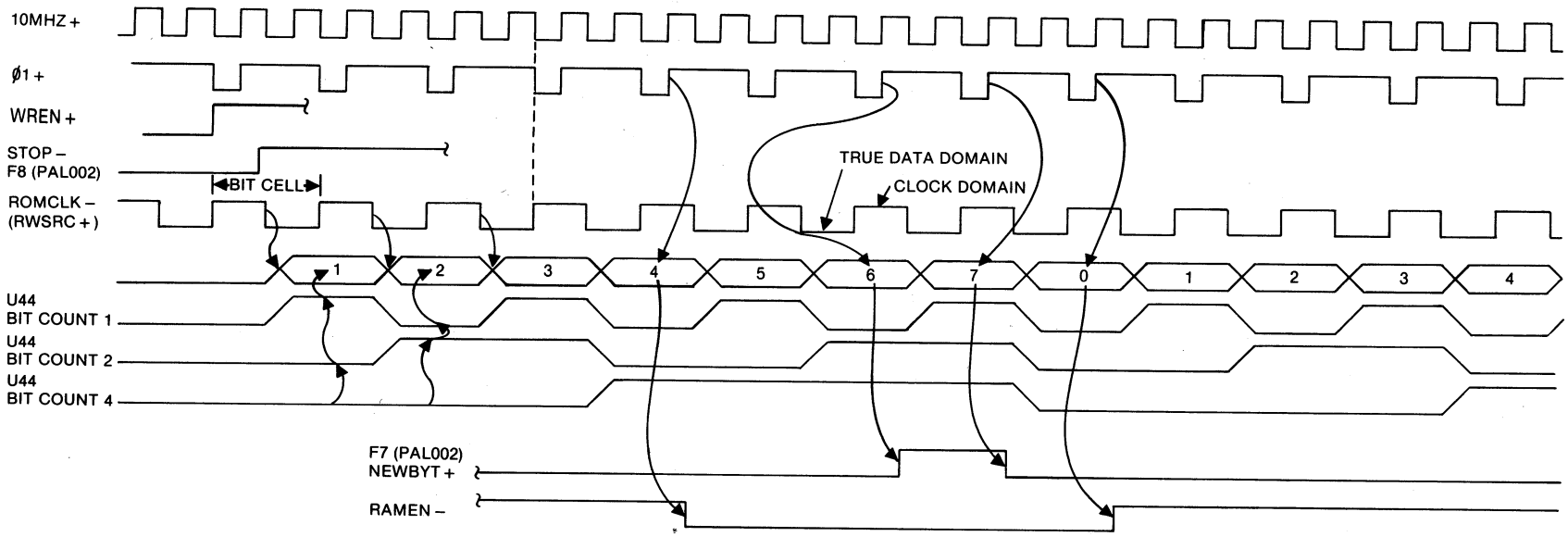


Figure 5-5. Write Timing PAL002

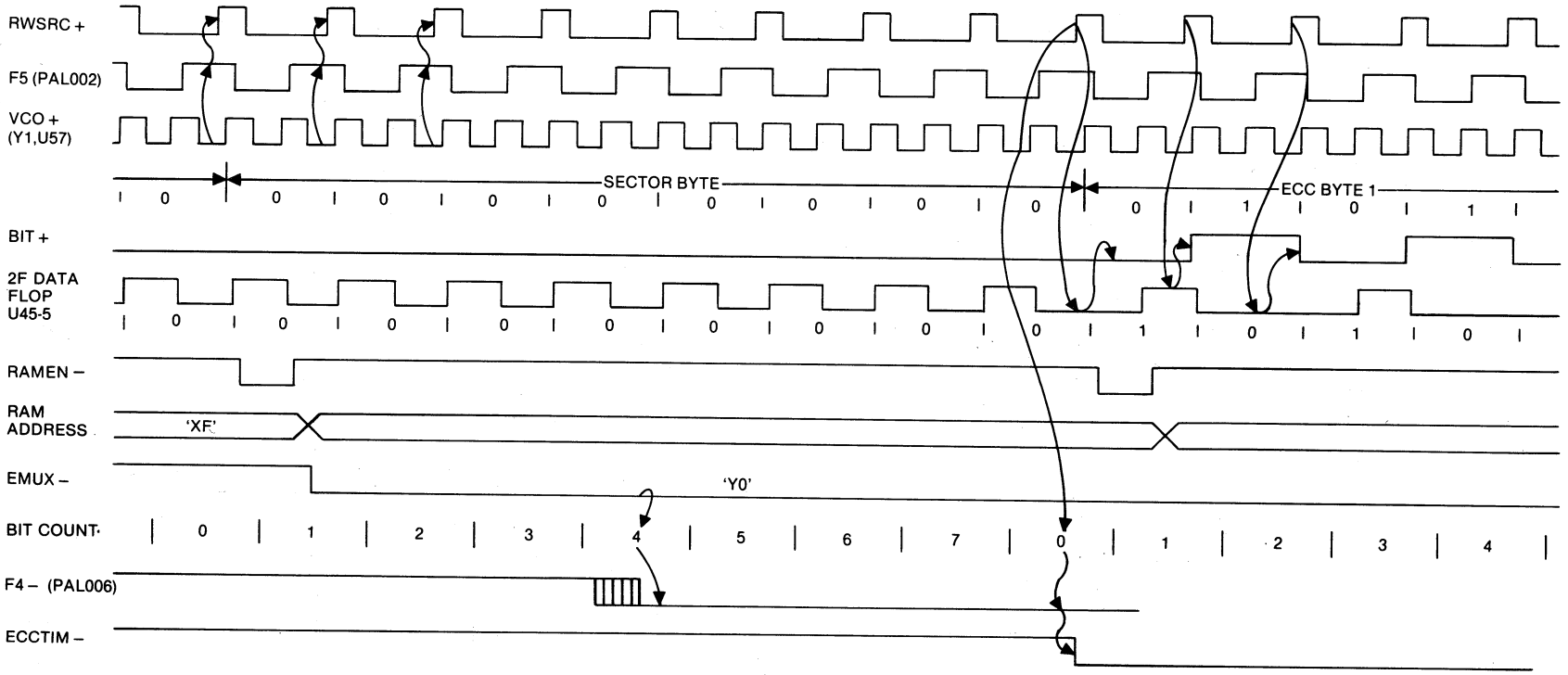


Figure 5-6. ECC Timing

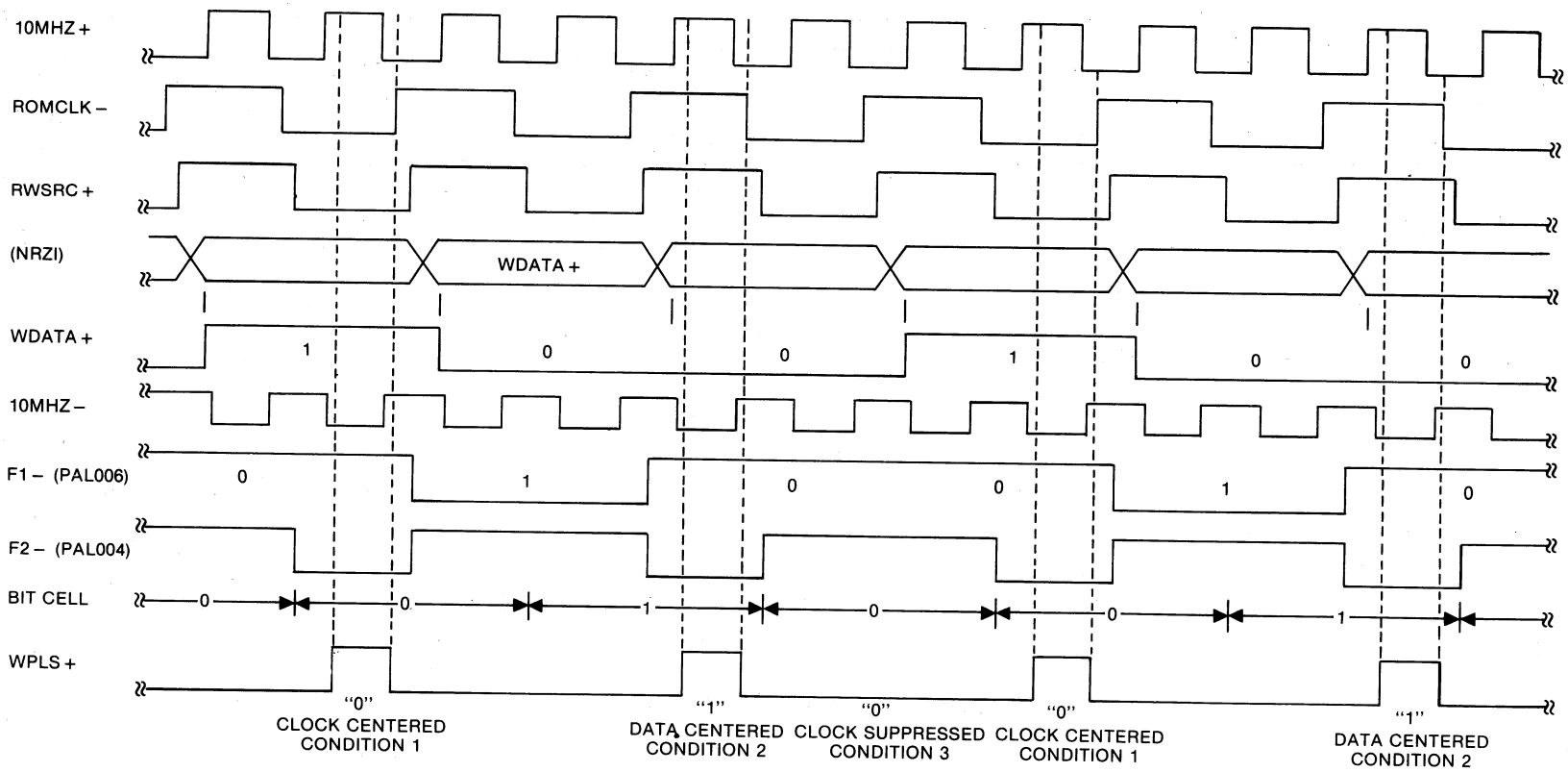


Figure 5-7. MFM Timing

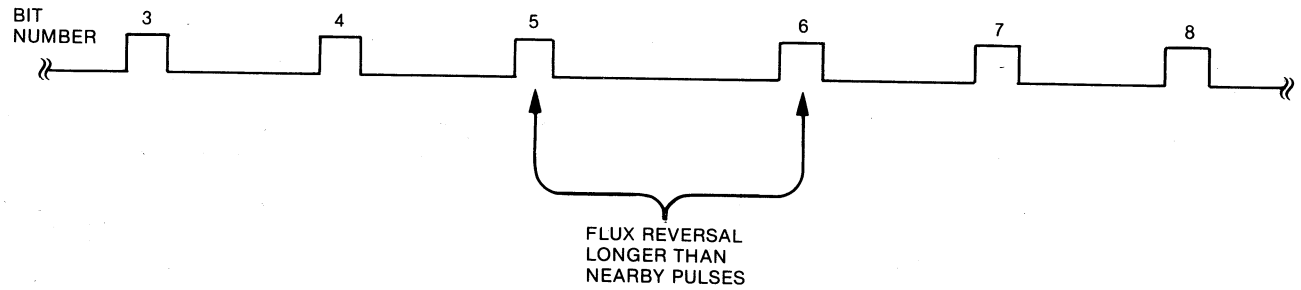


Figure 5-8. Peak Shift

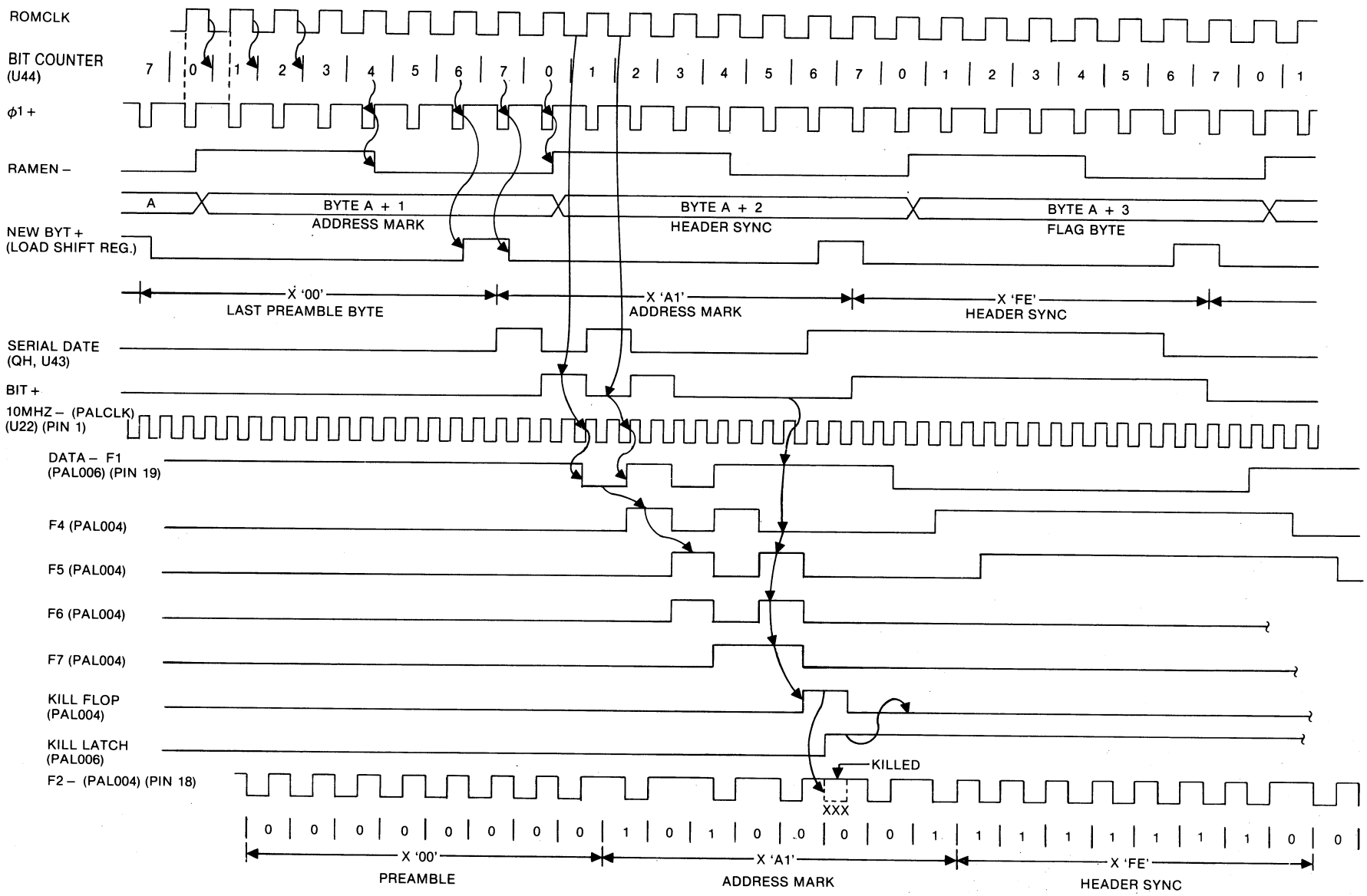


Figure 5-9. Address Mark and KILL Timing

Peripheral Interface – Read Data Path

A simplified diagram of the read data path is shown in Figure 5-10. The logic for read data inputs from the drive to the controller is shown on Sheet 10. The encoded pulse stream, RDAT0 for the first drive and RDAT1 for the second, are received by U7. Signals DRVSL0 and DRVSL1 are input to the U6 multiplexer selecting the drive and the pulse stream. The selected output of U6 is Y2, RMFM+, read modified frequency modulation. This signal is transmitted to the read/write multiplexer U57, Sheet 8.

The output Y2 of U57 is determined by read signals RMFM+ and AMSRCH (address mark search). When both are high, the CTCHME+ (catch me) signal is active. The latter is a pulse that is input to the phase-locked loop circuit where the controller timing "catches up" with the pulse stream.

Phase-Locked Loop – Read Data

The purpose of the phase-locked loop circuit, shown on Sheet 11, is to bring the timing on the controller in phase with data on the disc. A simplified diagram of the circuit is shown in Figure 5-11.

Component U47 is used at the input of the circuit as the temperature compensation reference. At the output, U47 is used for the analog conversion of phase difference. Because of temperature drift, both segments of the component change at approximately the same rate. The output of the compensation reference is transmitted to the *negative* input of the analog inverter, U58, and the output of the analog converter is transmitted to the *positive* input of U58. The analog inverter compares the phase error and the reference and corrects the voltage for the input of the voltage controlled oscillator, U35. The timing of the circuit, with and without phase error, is shown in Figures 5-12 and 5-13.

The term VCO+ is the output of the voltage controlled oscillator. The AMSRCH+ (address mark search) flip flop indicates that a read operation is taking place.

The term VCO+ is the clock input for the digitized phase difference flip flop, U46. This term and RDOS (read data one shot) determine the center of the phase as shown in the illustrations. If there is no phase error, the outputs of U47, which are PLS+ and PLS–, will be 55 nanoseconds each; both will be high and low for an equal time period.

As frequency of read data (RDOS) increases, PLS+ remains low longer, and PLS2– remains high for a shorter time, as shown in Figure 5-11. The exaggerated phase error shown in the example occurs when both PLS1+ and PLS2– are low for 76NS and high for 34NS. Notice that the 90NS high and low times are constant in both illustrations. The 110NS segment of the cycle is also constant; the trailing edges of PLS1+ and PLS2– shift left

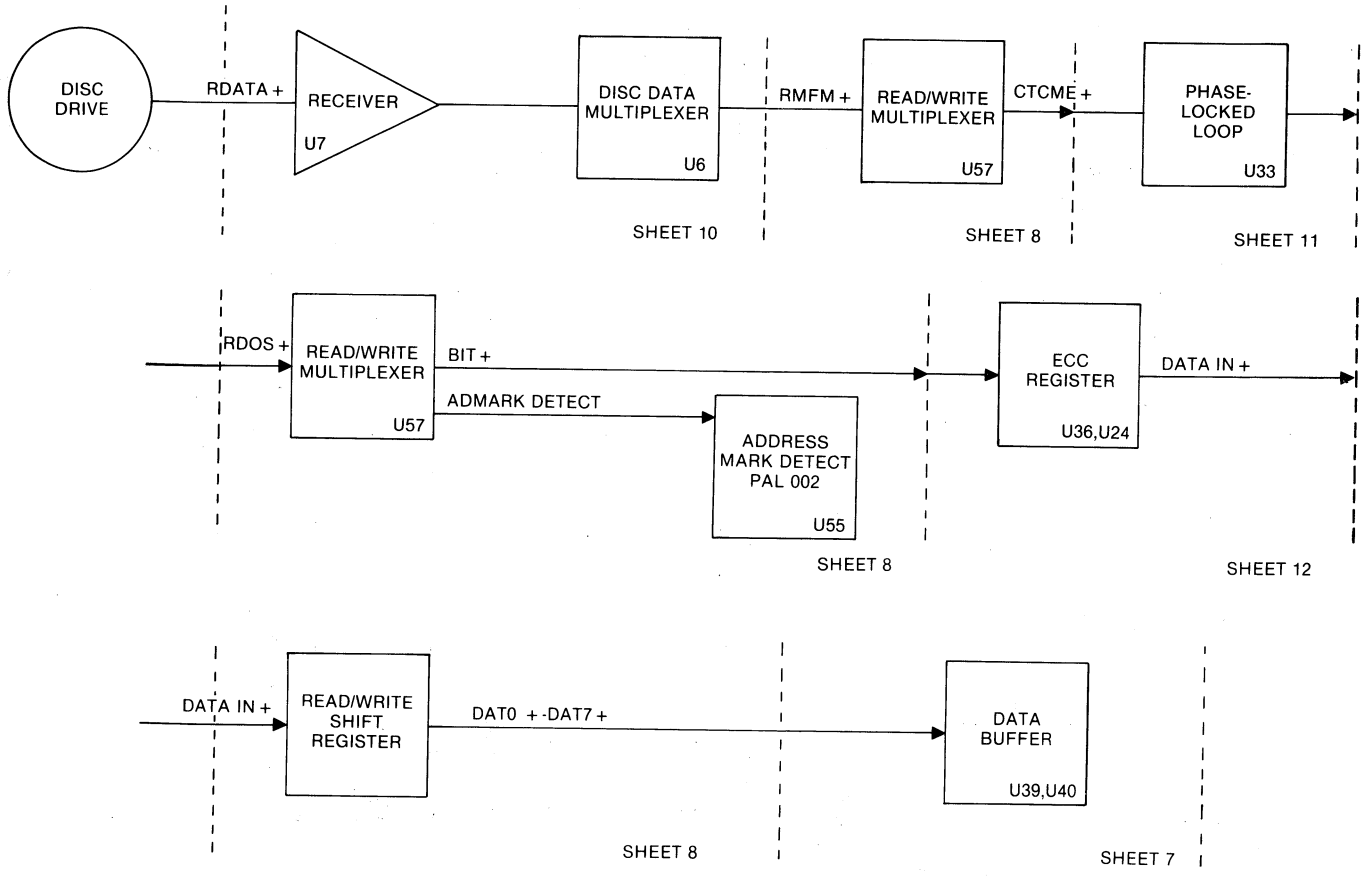


Figure 5-10. Read Data Path

relative to the center of this segment, whereas the leading edges of the pulses remain constant. This offset from center represents the phase error and is transmitted to the analog inverter, U58, where the voltage correction is made for the VCO. If the width of PLS2− is greater than PLS1+, RDOS is slower than the reference clock and must be phase shifted in the other direction.

ECC − Read

From the phase-locked loop circuit, RDOS is transmitted to DC flip flop U45 (pin 2), Sheet 8, where the signal is synchronized with the VCO signal. This signal is then selected by multiplexer U57 for a read operation and output at Y0, U57, to a second flip flop, U45 (pin 12). The latter flip flop acts

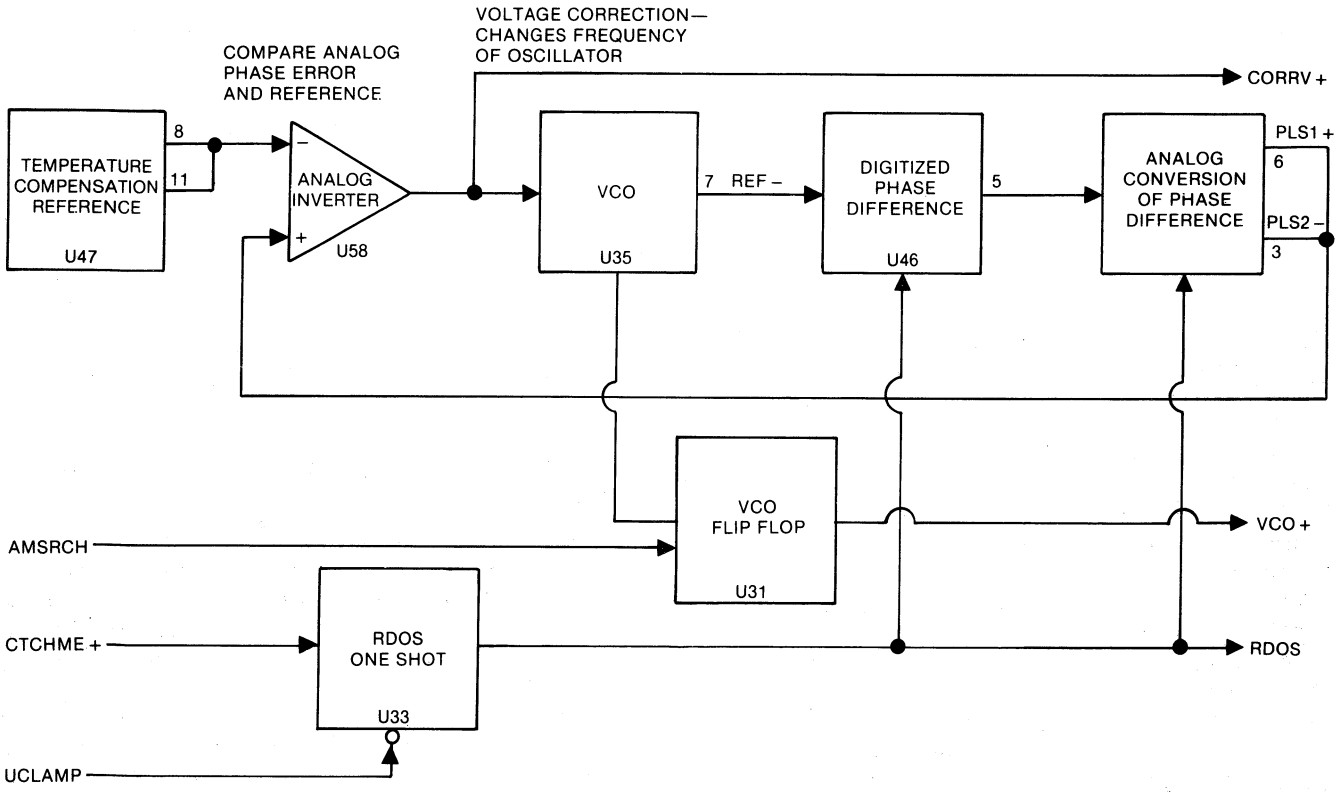


Figure 5-11. Simplified Diagram of Phase-Locked Loop

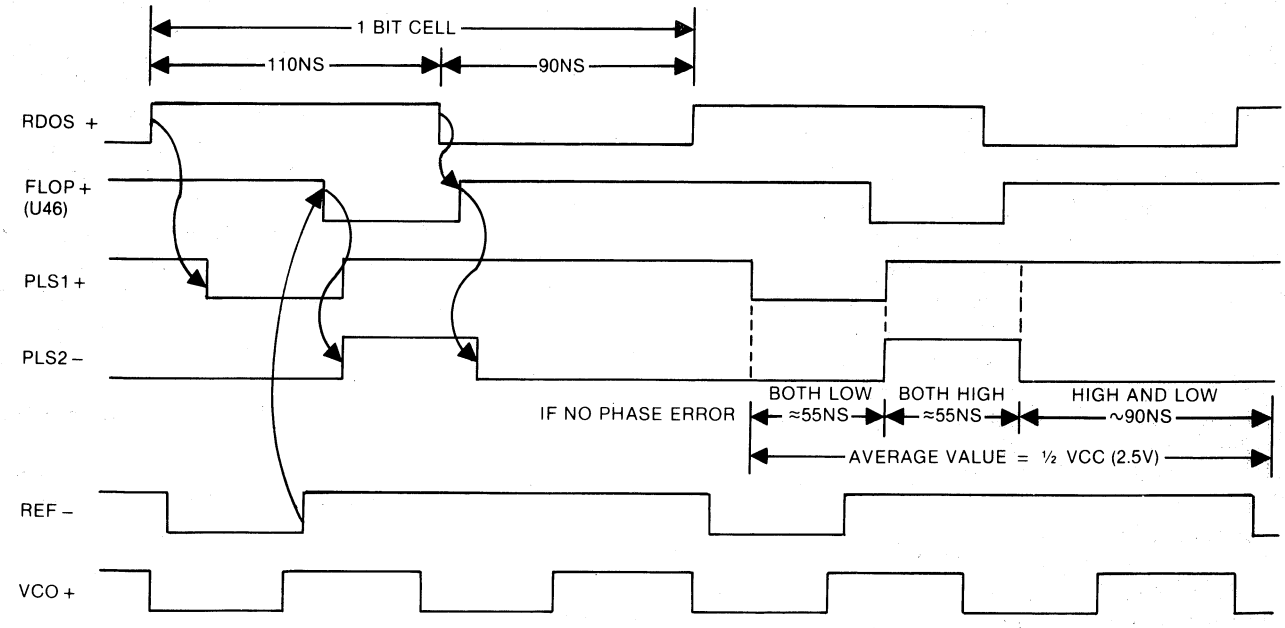


Figure 5-12. PLL Timing with No Phase Error

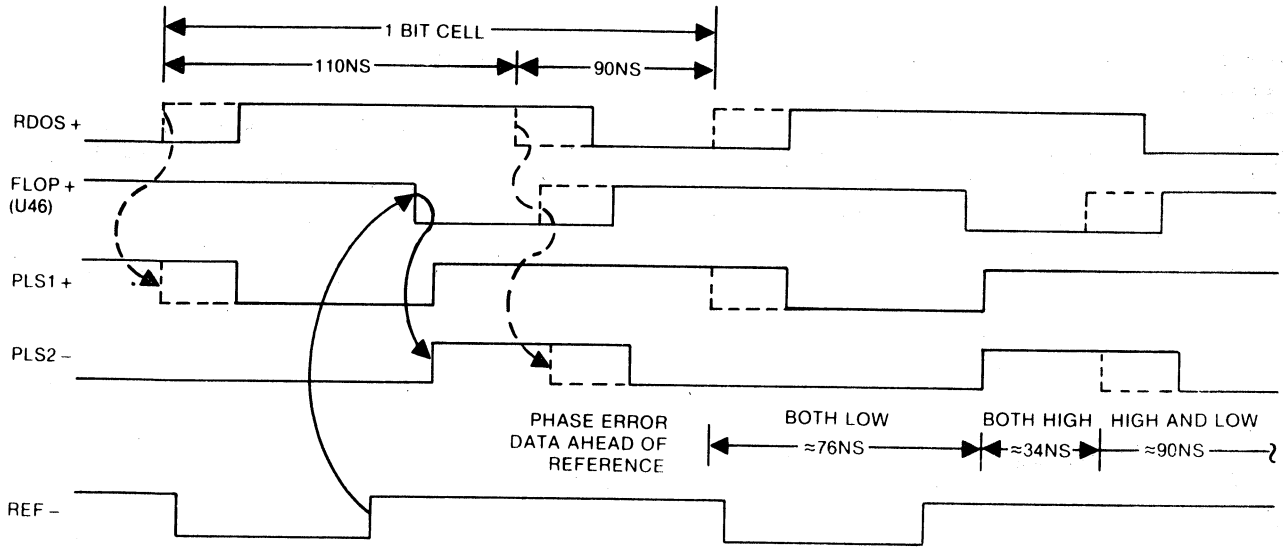


Figure 5-13. PLL Timing with Phase Error

as a holding bit, or ninth bit, to permit the ECC circuits to catch up with the rest of the logic. The output of this flip flop is BIT+ which goes to the ECC logic. The data stream is also transmitted to U55 (PAL002) from the first flip flop. This PAL is described below.

The ECC logic is shown on Sheet 12. BIT+ is transmitted to the parity generator, U36, and to multiplexer U24. The components U37, U48, U49 and U50 are 8-bit serial-in, parallel-out shift registers. These components divide data from the disc and generate a 32-bit remainder word. If the remainder is not zero, a "syndrome" is created. If the remainder is equal to zero, there is no error. The output of U36, pin 5, is the even sum of the 32-bit parity generator. Odd parity from U36, pin 6, to U24, Y3 is output to flip flop U53. The flip flop monitors the 32-bit syndrome. If there are zero's output from the flip flop there is no error, and the output ECCERR+ is false. If there is an error, then ECCERR+ is true.

When ECCTIM– is a high signal to U24, the output Y0 reads BIT+. When ECCTIM goes low Y0 reads from the parity generator through switch 1. At ECC time, the pulse stream becomes the syndrome and is read into the data buffer right behind the data from the disc. The data and syndrome (DATAIN+) are read into the microcode to determine if the error is correctable or uncorrectable.

When Switch 1 is OFF (open), the syndrome is discarded, and from Y0, thirty-two 1's will flag the controller that the error is uncorrectable. The switch is used when running diagnostics so that media flaws can be detected and mapped. When the switch is ON (closed), a valid syndrome is transmitted to the RAM.

The signal CP6– resets the ECC register and error flip flop. The signal ECCEN+ is active when ECC time is false. This term from Y1 enables U48. The signal prohibits extraneous pulses from being entered into the ECC polynomial, e.g., address mark or sync pulses.

The signal DATAIN+ is transmitted to the read/write shift register (Sheet 8) for parallel transfer to the data buffer.

Address Mark Detect and Byte Clock Control – Read

The logic for address mark detect is shown on Sheet 8. As serial data (DATAIN+) is transmitted to the shift register, the data stream from the phase-locked loop circuit (RDOS) is transmitted to PAL002, address mark detect, through flip flop U45, pin 5.

The outputs of PAL002 flip flops F1, F2, F3 and F4 are used to form a four bit state machine that scans the incoming data stream from the U45 flip flop for the unique pattern of the address mark character. When the address mark is detected, the flip flops lock into hexidecimal state 'F' (1111). Flip flop F5 is used to detect the locking action of the state machine and will begin to toggle when this occurs. F5 is then used to divide the VCO clock in half and be synchronized to the data domain of the incoming data stream. F6 is used to control the RAM buffer cycling on read/write commands. This timing relationship is shown in Figure 5-14. At bit count 8, F6 is stable 1 bit time to enable one byte from the shift register to be input to the RAM.

The output F5 from the pal is a 5 MHz clock gated (U11, pin 2) with the 10 MHz VCO clock (U11, pin 1). The resulting signal (U11, pin 3) is a 5 MHz clock in the middle of the data domain, which goes to B3 of the multiplexer and is output (Y3) to the 3-bit counter U44.

The flip flop F7 is used during a write operation. F8 (STOP–) indicates that the read/write operation is complete, and this is transmitted to the microcode.

Clocks

The controller clock logic is shown on Sheet 13. The timing relationship is shown in Figure 5-15.

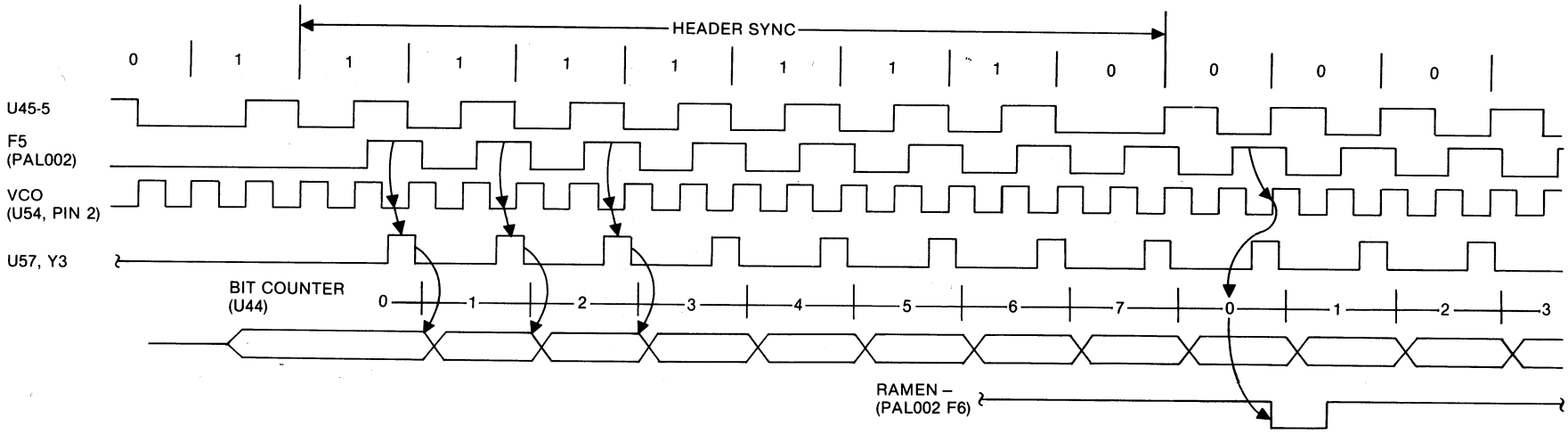


Figure 5-14. Byte Clock Control

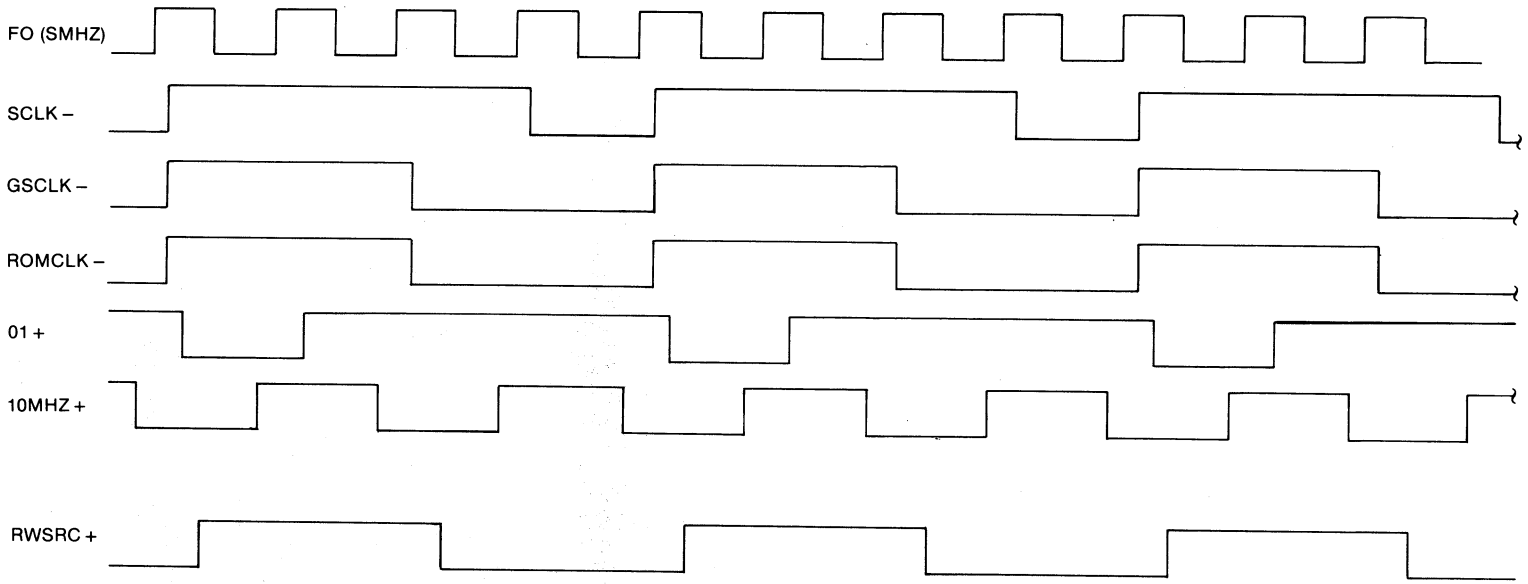
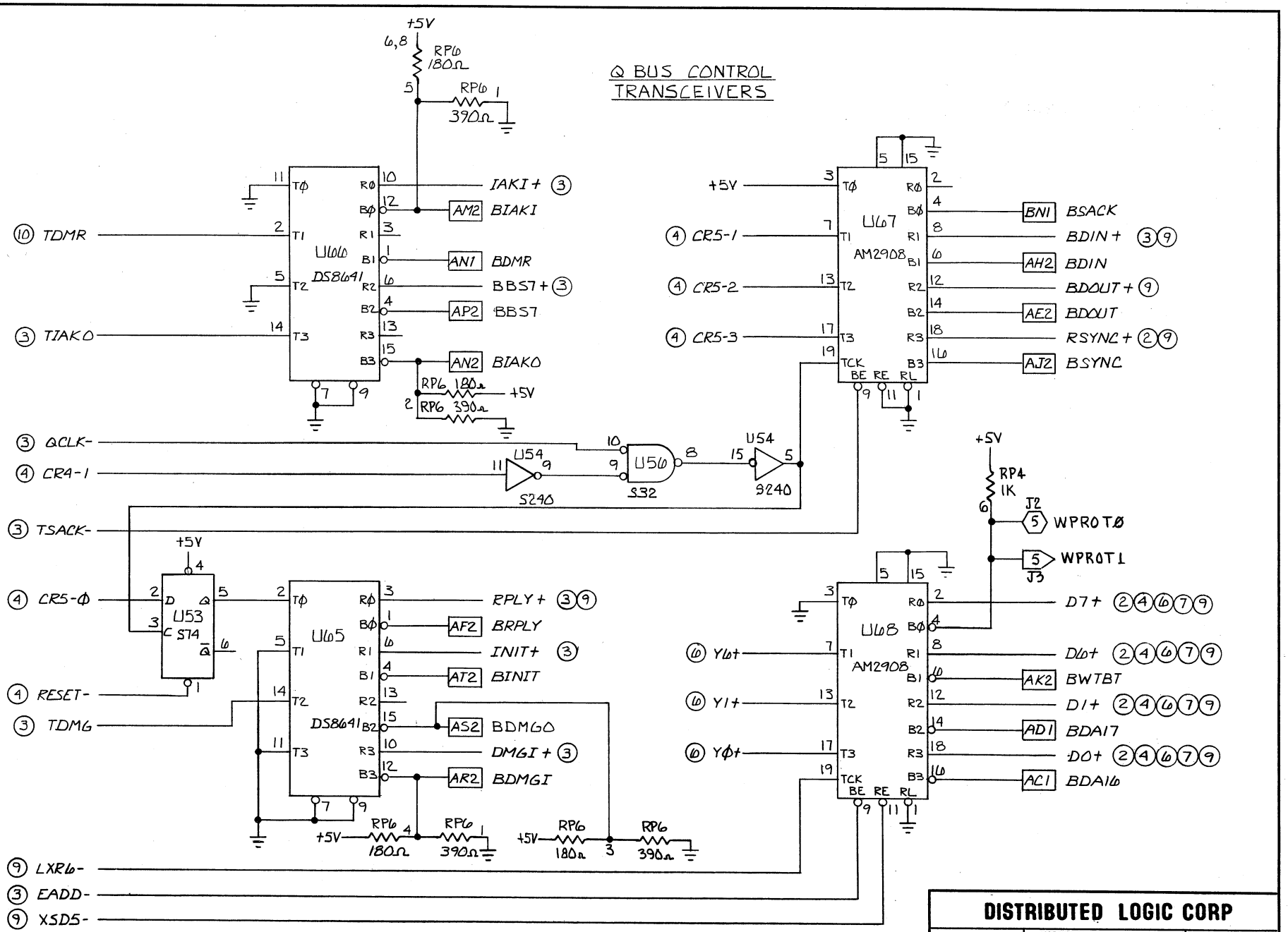


Figure 5-15. Clocks



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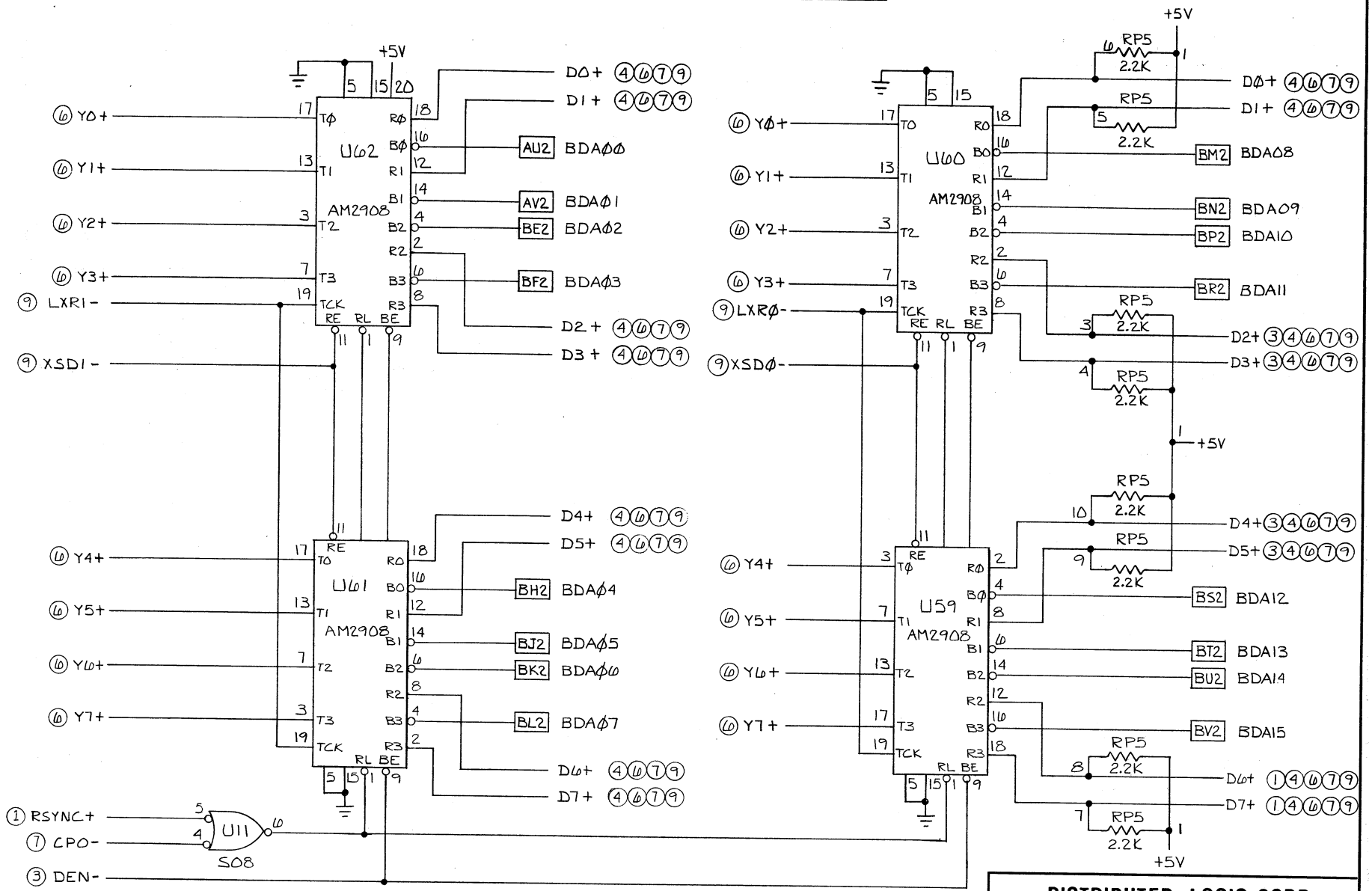
LOGIC DIAGRAM DQØ14		SHT 1 OF 13
		DRAWING NUMBER 853040 C

DATA/ADDRESS TRANSCEIVERS



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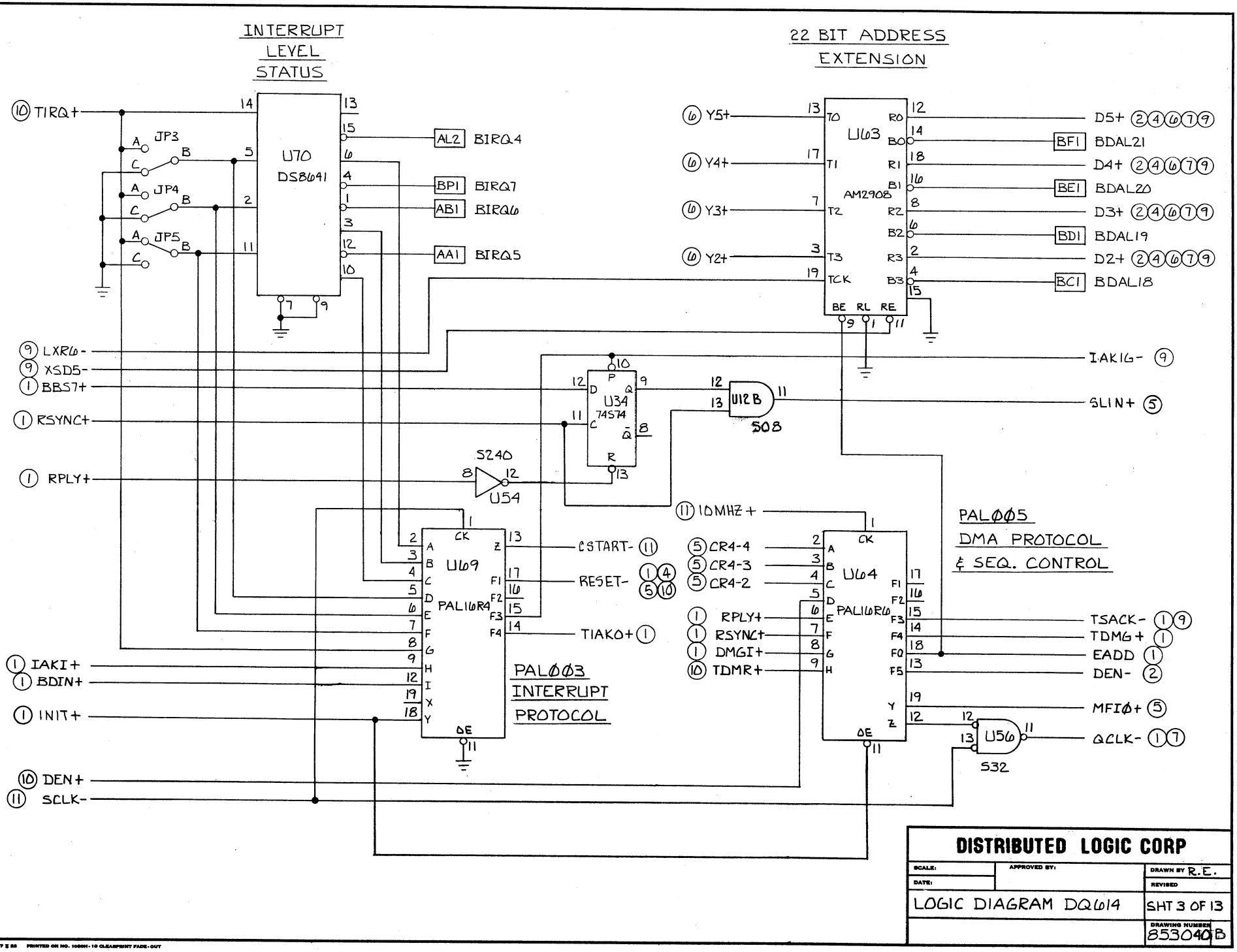
INTERRUPT LEVEL STATUS
22 BIT ADDRESS EXTENSION
U70 DS8641
JP3
JP4
JP5
U63 AM2908
U34 74S74
U112B S08
S240 U54
U69 PAL16R4
U64 PAL16R6
U56 S32
PAL Ø Ø 5 DMA PROTOCOL & SEQ. CONTROL
PAL Ø Ø 3 INTERRUPT PROTOCOL
TIRQ+
AL2 BIRQ4
BP1 BIRQ7
AB1 BIRQ6
AA1 BIRQ5
Y5+
Y4+
Y3+
Y2+
D5+ 2 4 6 7 9
BF1 BDAL21
D4+ 2 4 6 7 9
BE1 BDAL20
D3+ 2 4 6 7 9
BD1 BDAL19
D2+ 2 4 6 7 9
BC1 BDAL18
LXRQ-
XSD5-
BBS7+
RSYNC+
RPLY+
IAKIG- 9
SLIN+ 5
10MHZ+
CSTART- 11
RESET- 1 4 5 10
TIAKO+ 1
CR4-4
CR4-3
CR4-2
RPLY+
RSYNC+
DMGI+
TDMR+
TSACK- 1 9
TDMG+ 1
EADD 1
DEN- 2
MFIØ+ 5
QCLK- 1 7
IAKI+
BDIN+
INIT+
DEN+
SCLK-
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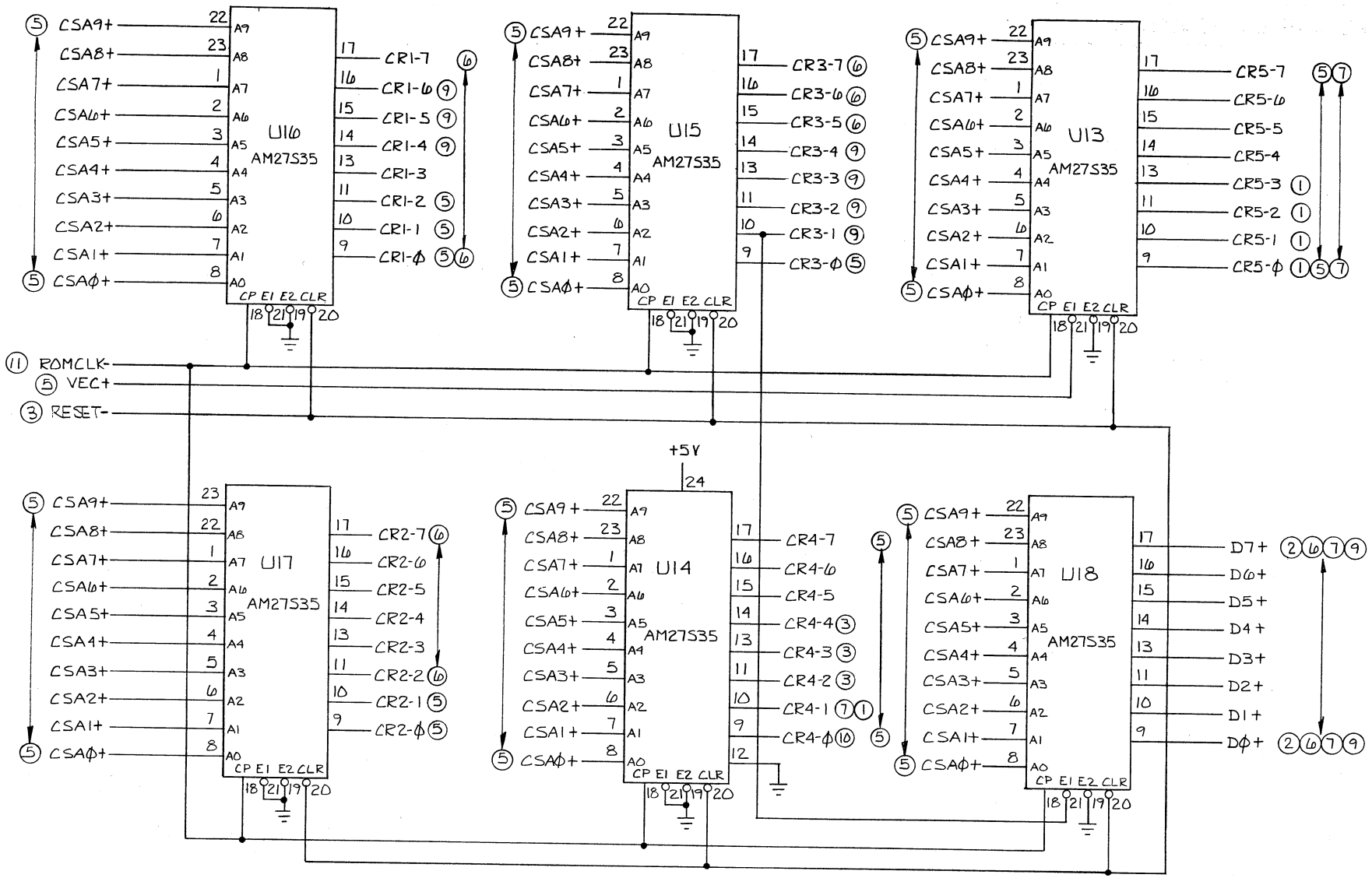
MICROPROGRAM MEMORY



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LOGIC DIAGRAM DQ6014		SHT 4 OF 13
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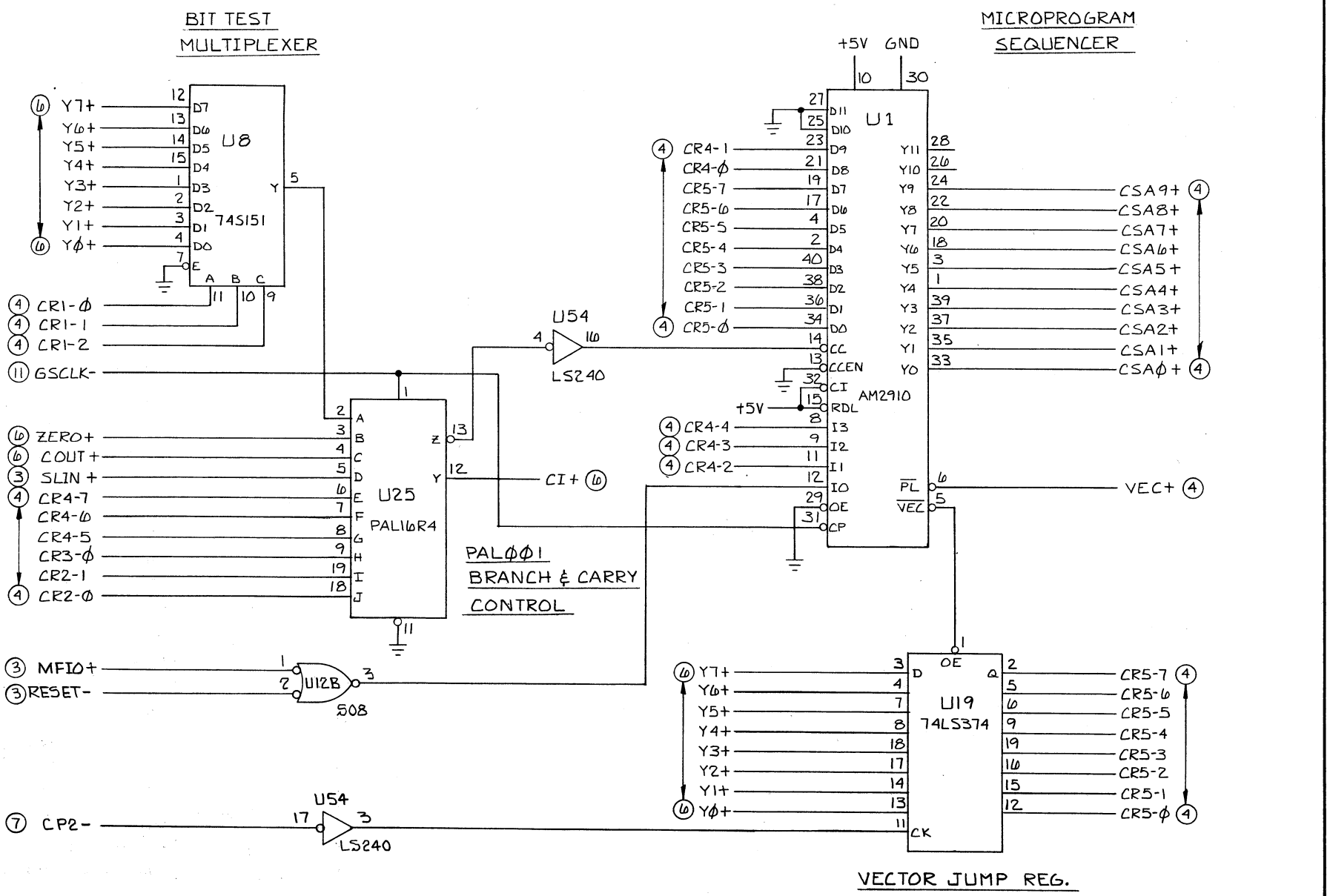
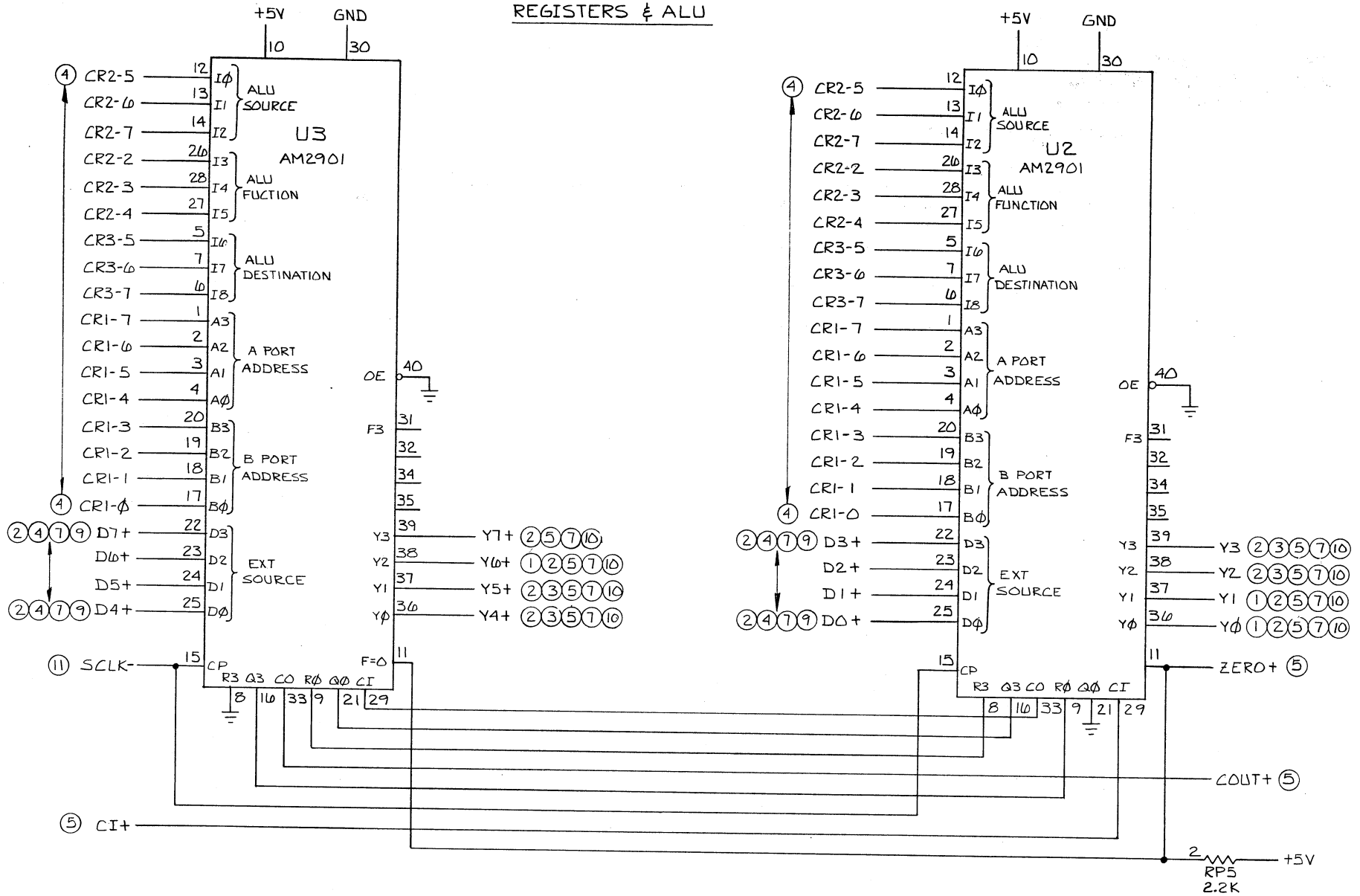


REGISTERS & ALU



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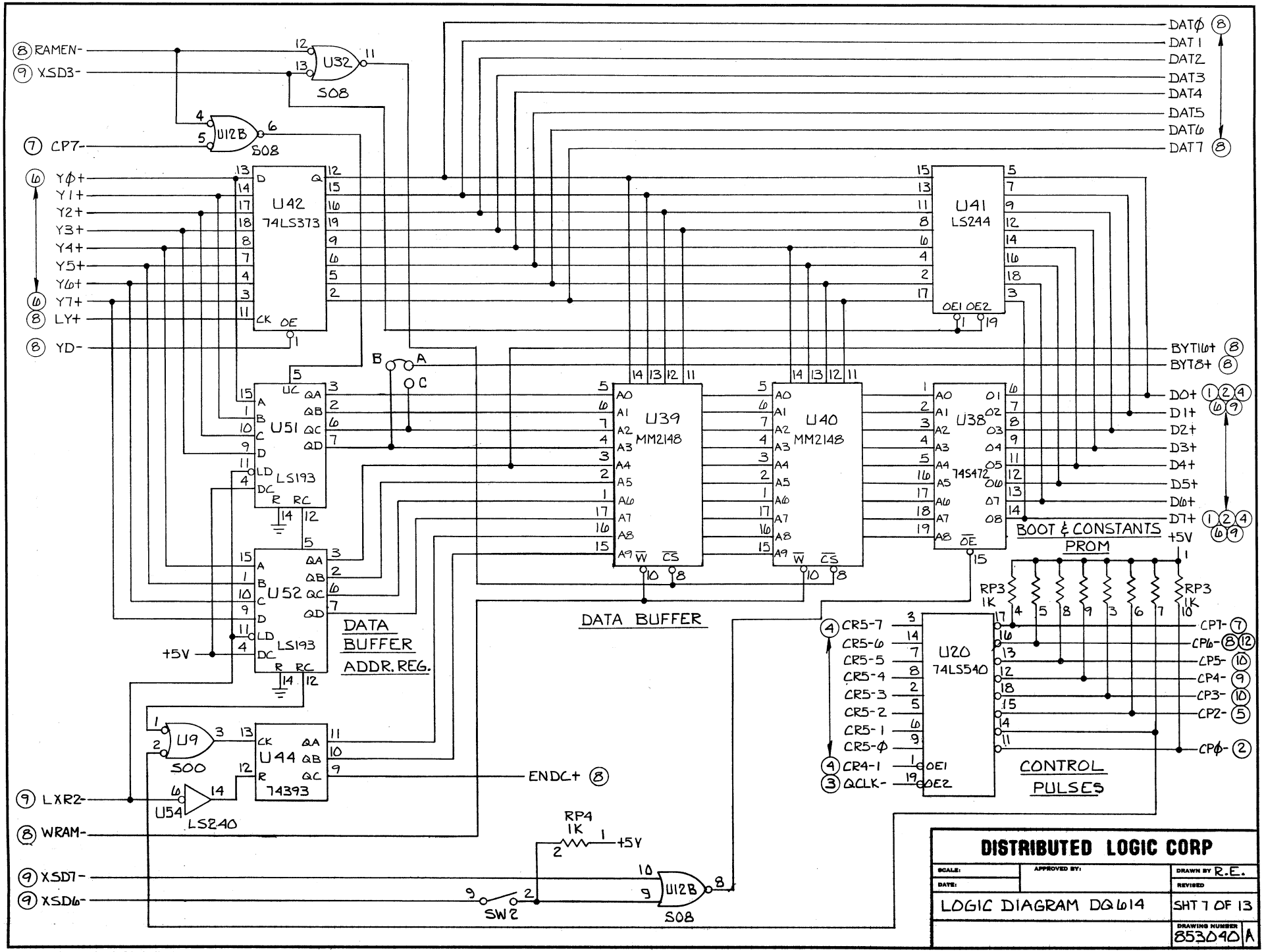

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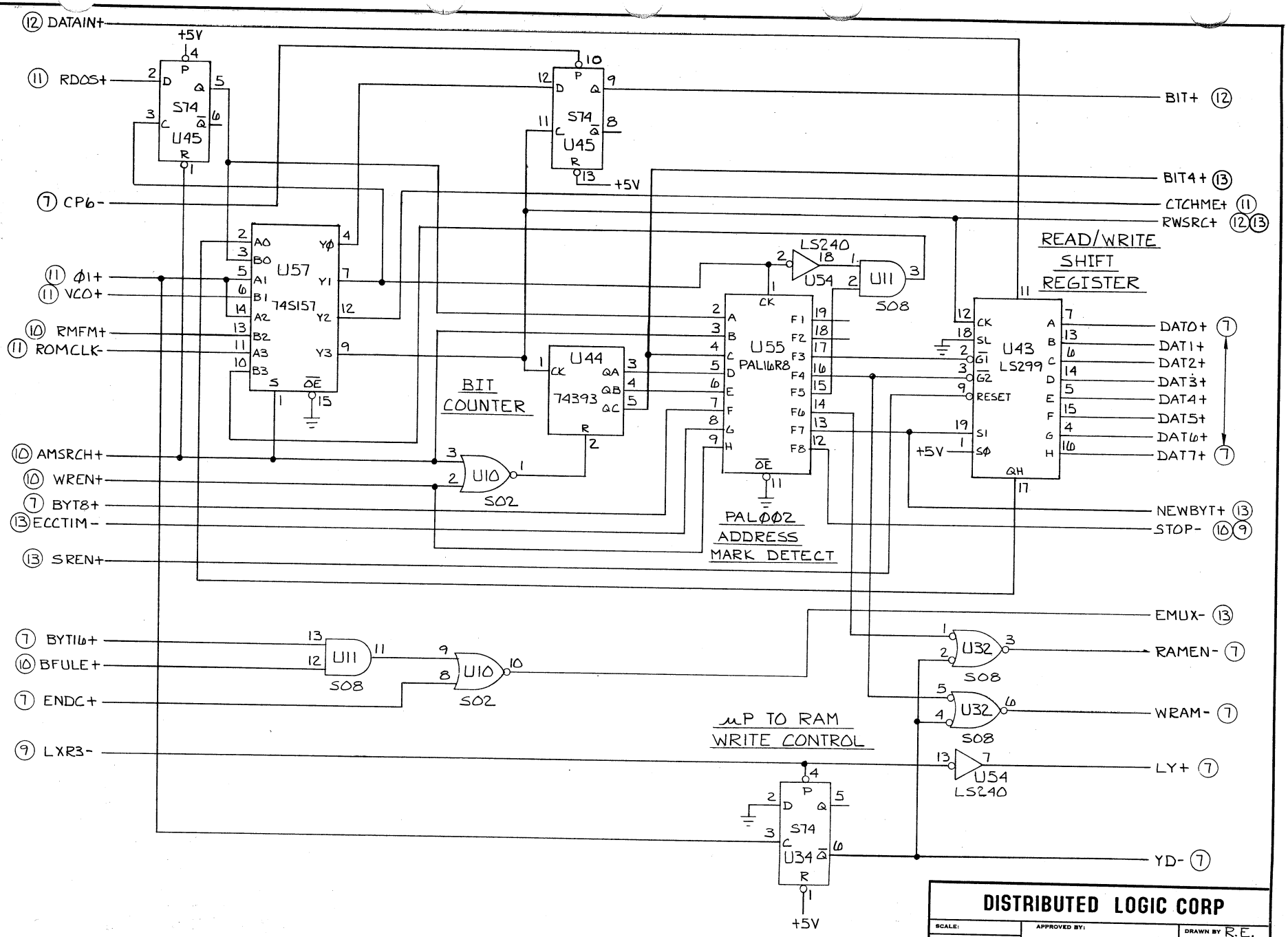
(12) DATAIN+
+5V
(11) RDOS+
U45
S74
(7) CP6-
BIT+ (12)
BIT4+ (13)
CTCHME+ (11)
RWSRC+ (12)(13)
READ/WRITE SHIFT REGISTER
U57
74S157
(11) Φ1+
(11) VCO+
(10) RMFM+
(11) ROMCLK-
U44
74393
BIT COUNTER
LS240
U54
U11
S08
U55
PAL16R8
PALØØ2 ADDRESS MARK DETECT
U43
LS299
DAT0+ (7)
DAT1+
DAT2+
DAT3+
DAT4+
DAT5+
DAT6+
DAT7+ (7)
(10) AMSRCH+
(10) WREN+
(7) BYT8+
(13) ECCTIM-
U10
S02
NEWBYT+ (13)
STOP- (10)(9)
(13) SREN+
EMUX- (13)
(7) BYTI6+
(10) BFULE+
(7) ENDC+
U32
RAMEN- (7)
WRAM- (7)
(9) LXR3-
μP TO RAM WRITE CONTROL
LY+ (7)
U34
YD- (7)
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LOGIC DIAGRAM DQ614
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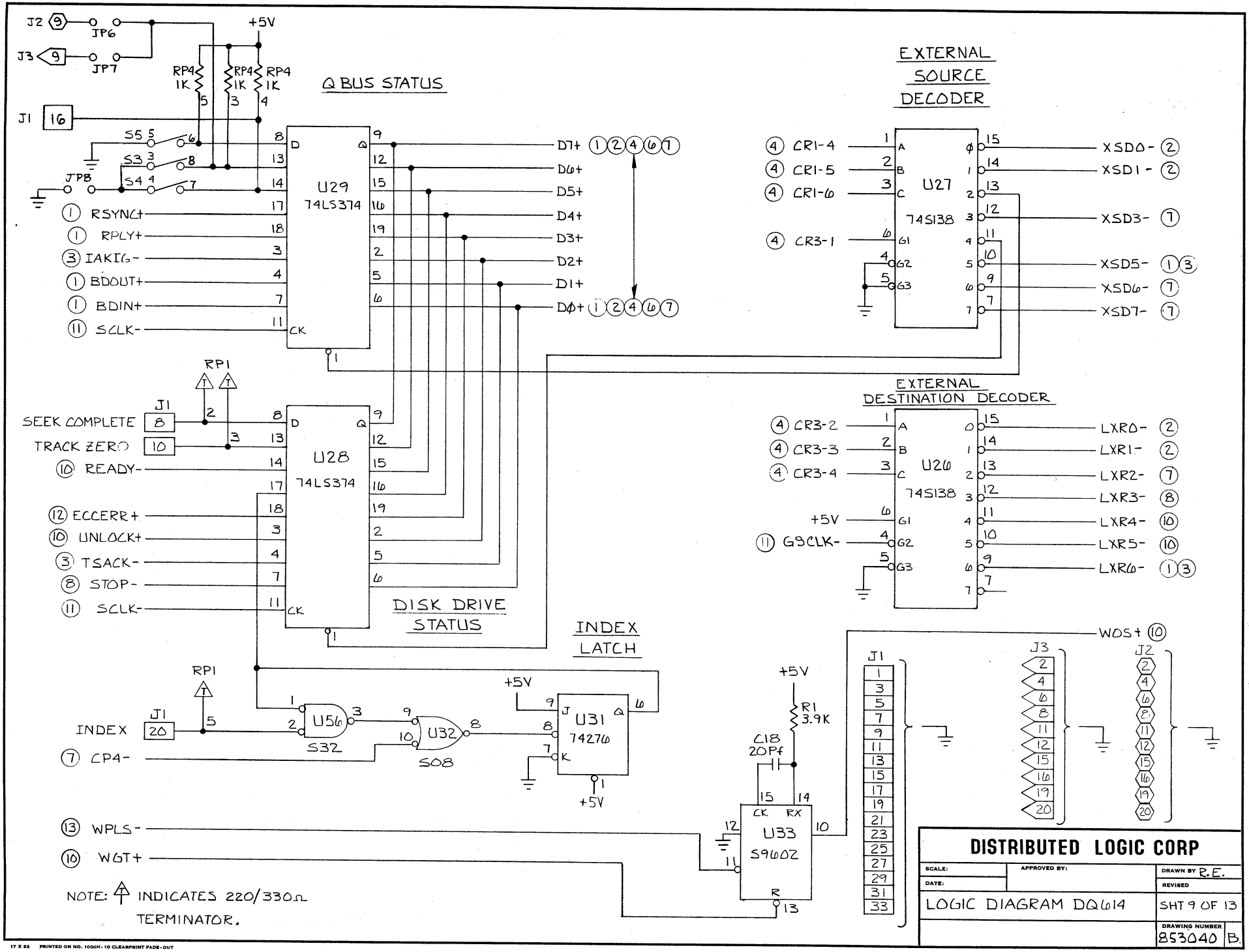
17 X 22 PRINTED ON NO. 1000H-10 CLEARPRINT FADE-OUT



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LOGIC DIAGRAM DQ614	SHT 9 OF 13
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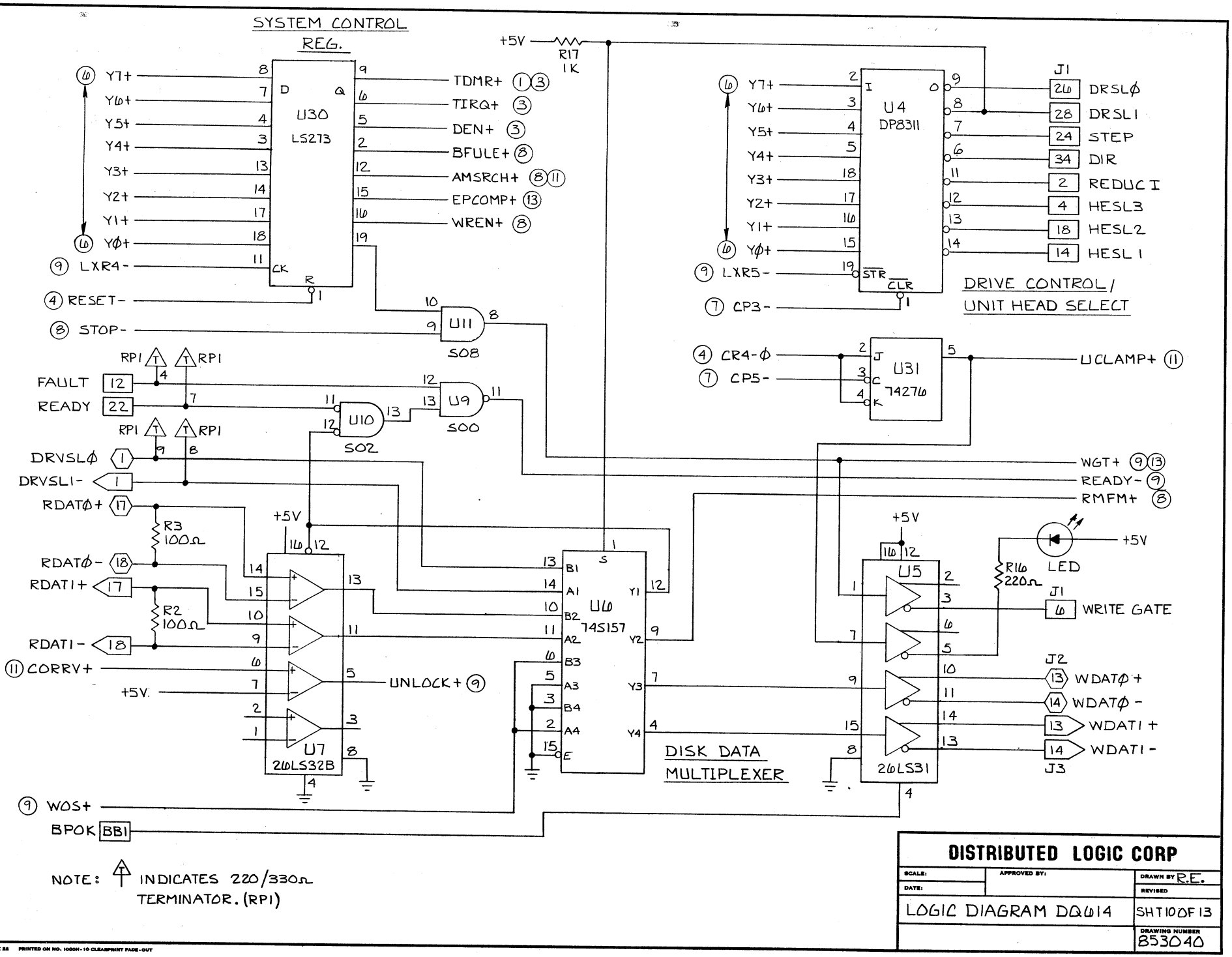

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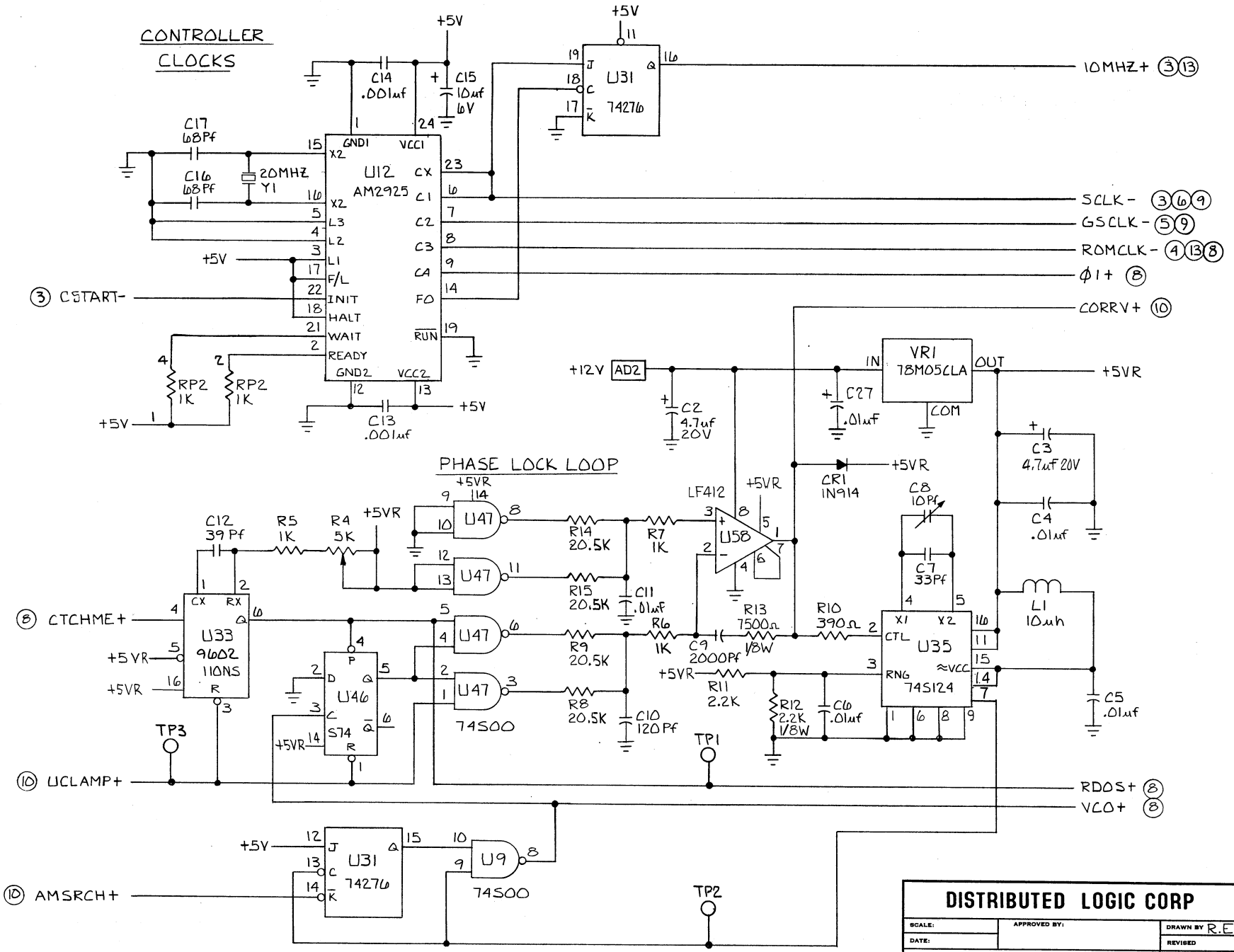

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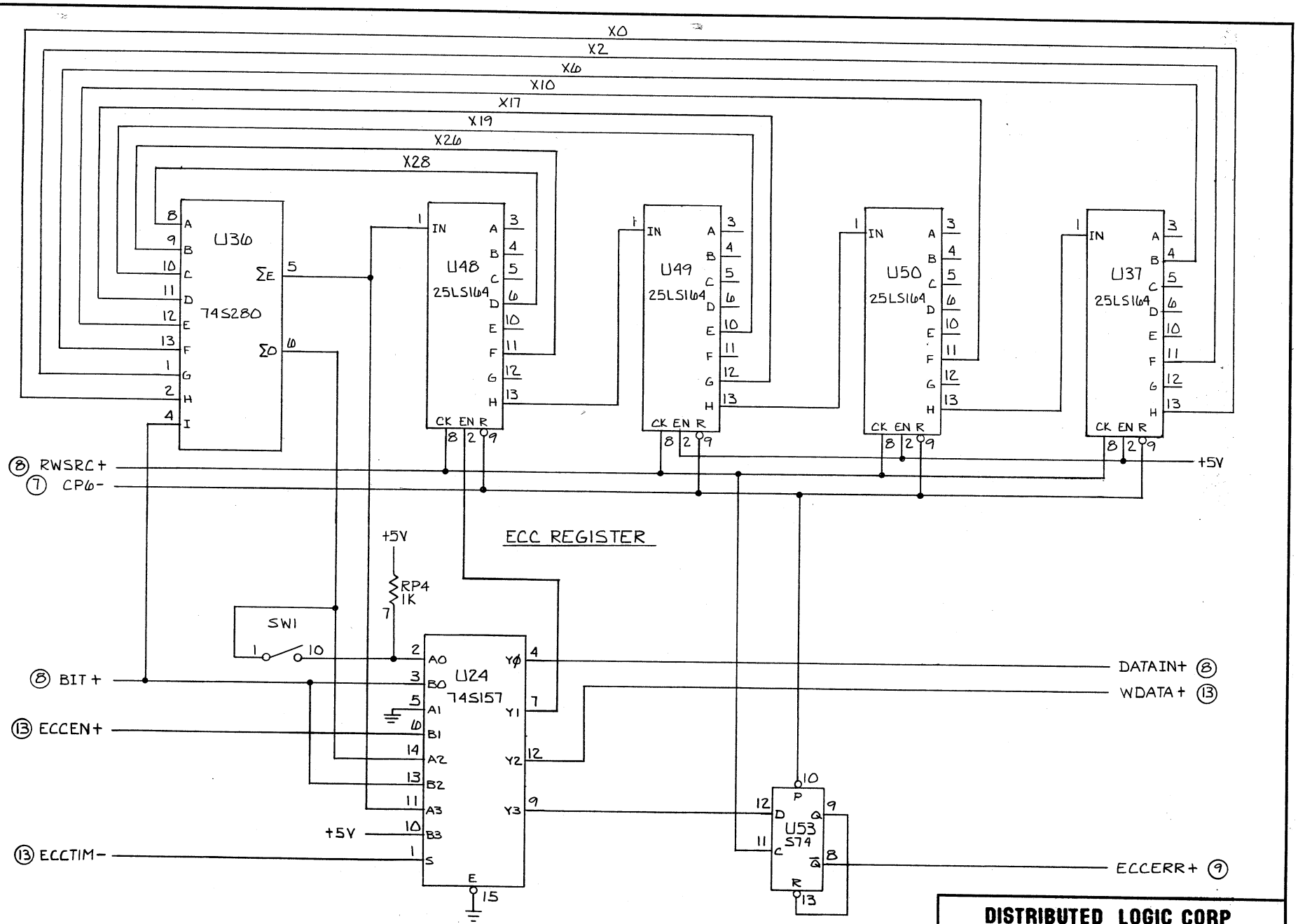

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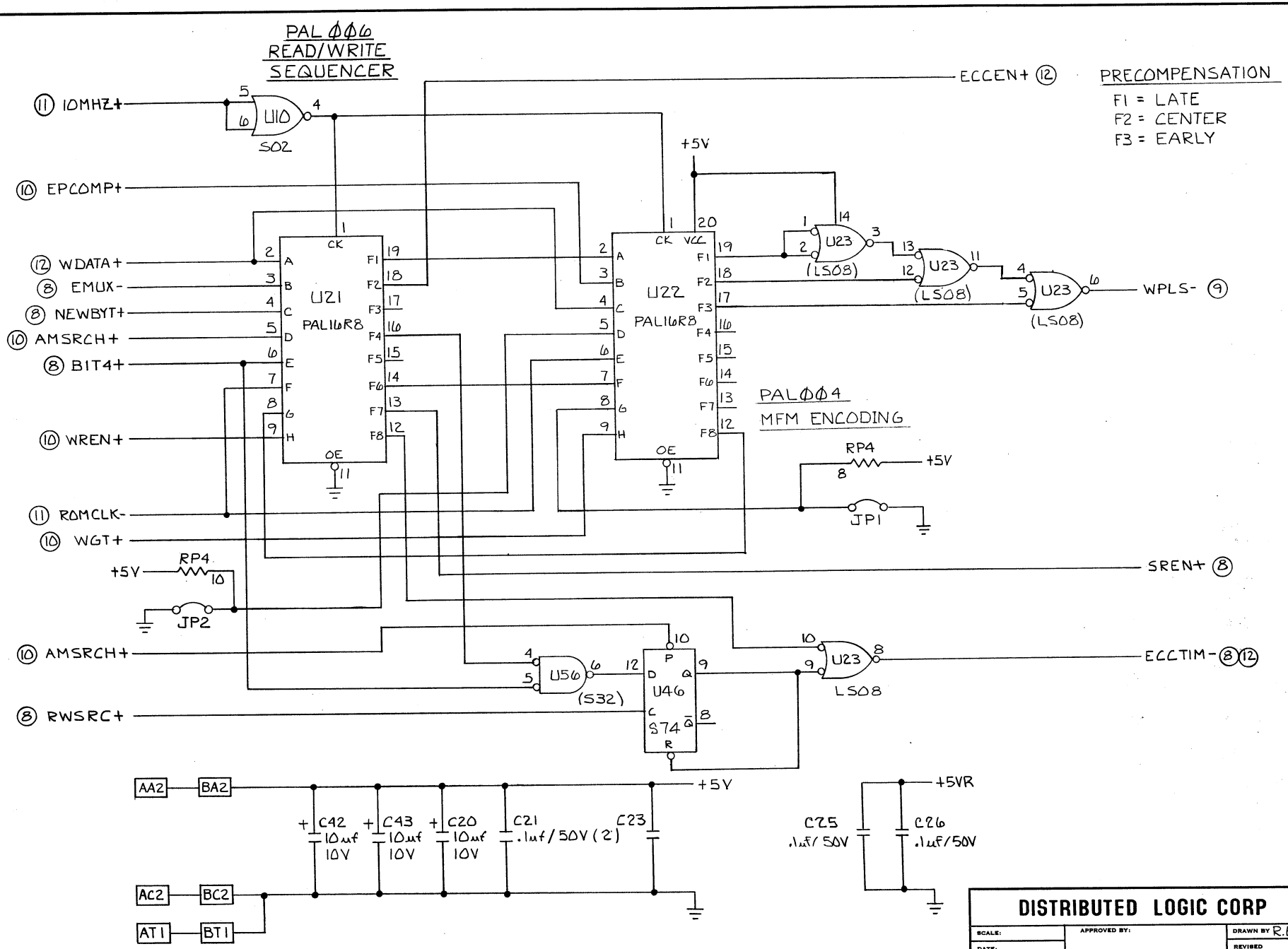

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