EK-PS730-TD-001

H7202B Power System Technical Description

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H7202B Power System Technical Description

Prepared by Educational Services
of
Digital Equipment Corporation

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CHAPTER 1
INTRODUCTION

1.1 SCOPE

This manual presents the technical description of the H7202B power supply configured for use with the VAX-11/730, including its components and the relationship between them.

1.2 GENERAL DESCRIPTION

The H7202B power supply consists of:

- AC Input Assembly (7018136-00)
- (H7200) +5.1 V Power Module
- (H7211) Communications Power Module
- (H7213) Memory Power Module
- (H7202) Output Distribution Board (5413877-00)

1.2.1 AC Input Assembly (7018136-00)

The AC input assembly is the medium between the input power (115 Vac or 230 Vac and BBU power) and the H7200. The ac input assembly consists of a line filter to block high frequency disturbance from either direction on the ac line, a line voltage select switch (S1) to select the proper input voltage, and a 15 ampere circuit breaker (CB1) to protect the ac input source against possible power supply overcurrents.

1.2.2 (H7200) +5.1 V Power Module

The H7200 employs

- a voltage doubler/rectifier to convert ac input power to the +/−150 volt bulk dc.
- a pulse width modulated flyback converter to convert the bulk dc to the +/−14 Vdc internal low voltage (ILV).
- a pulse width modulated forward converter to convert the bulk dc to the regulated +5.1 V, 60 A output.

Also employed is logic and control circuitry to monitor, control, and indicate power supply status. The H7200 also generates the 33 kHz power supply synchronization pulses.

1.2.3 (H7211) Communications Power Module

The H7211 uses a pulse width modulated flyback converter to convert the bulk dc to the regulated −15 V, 3 A and +15 V, 2 A outputs.

1.2.4 (H7213) Memory Power Module

The H7213 uses a pulse width modulated forward converter to convert the bulk dc to the regulated +5.1 V, 15 A and +12.3 V, 3 A outputs.

1.2.5 (H7202) Output Distribution Board (5413877-00)

The output distribution board is the interface between the power supply and the VAX-11/730 for all input control signals and output voltages (excluding the +5.1 V, 60 A output) and signals.

1.3 CONTROLS AND INDICATORS

The controls and indicators on the H7202B power supply and their functions are listed in Table 1-1.

Table 1-1 H7202B Power Supply Controls and Indicators

Control/Indicator	Function
Line Voltage Select Switch	Selects the AC input voltage to be used.
Circuit Breaker	Protects the AC line against faults in the power supply.
CH 1 Indicator	Indicates the H7200 output is within regulation when lit.
CH 2 Indicator	Indicates the H7211 outputs are within regulation when lit.
CH 3 Indicator	Indicates the H7213 outputs are within regulation when lit.

1.4 RELATED DOCUMENTATION

1.4.1 VAX-11/730 Technical Documentation

The documentation listed in Table 1-2 describes the operation of the basic VAX-11/730 system.

Table 1-2 Related Documentation

Title	Document Number
VAX-11/730 Central Processor Unit Technical Description	EK-KA730-TD
VAX-11/730 Memory System Technical Description	EK-MS730-TD
FP730 Floating-Point Accelerator Technical Description	EK-FP730-TD
VAX-11/730 Integrated Disk Controller Technical Description	EK-RB730-TD
VAX-11/730 System Maintenance Guide	EK-11730-MG
VAX Diagnostic System User's Guide	EK-VX11D-UG
VAX-11/730 Diagnostic System Overview Manual	EK-DS730-UG
VAX-11/730 System Installation Guide	EK-SI730-IN
VAX-11/730 Hardware User's Guide	EK-11730-UG
VAX Architecture Handbook	EB-21811
VAX Hardware Handbook	EB-21710
VAX System Site Preparation Guide	AE-20190
VAX-11/730 Customer Installation Guide	EA-21160
DMF32 Multi-Function Communications Technical Description	EK-DMF32-TD
VAX-11/730 Illustrated Parts Breakdown	EK-11730-IP

1.4.2 Field Maintenance Print Set

The engineering drawings of the field maintenance print set applicable to the H7202B power supply are listed in Table 1-3.

Table 1-3 Engineering Drawings for the H7202B Power Supply

Title	Document Number
H7202 Power Supply	E-UA-H7202-0-0
H7202 Power Supply Parts List	K-PL-H7202-0-DBP
H7202B Interconnect	D-IC-H7202-0-2
5 V Power Module	D-UA-H7200-0-0
5 V Power Module	K-PL-H7200-0-DBP
Communications Power Module	B-UA-H7211-0-0
Communications Power Module	K-PL-H7211-0-DBP
Memory Power Module	B-UA-H7213-0-0
Memory Power Module	K-PL-H7213-0-DBP
H7202 Box Assembly	E-AD-7017635-0-0
H7202 Box Assembly	K-PL-7017635-0-DBP
AC Power Assembly	D-AD-7017636-0-0
AC Power Assembly	K-PL-7017636-0-DBP
Output Assembly (H7200)	D-AD-7017638-0-0
Output Assembly (H7200)	K-PL-7017638-0-DBP
Major Board (+5V60A)	D-UA-5413857-0-0
Major Board (+5V60A)	K-PL-5413857-0-DBP
Major Board (+5V60A)	D-CS-5413857-0-1
Memory Reg Board (+5V)	E-UA-5413869-0-0
Memory Reg Board (+5V)	K-PL-5413869-0-DBP
Memory Reg Board (+5V)	D-CS-5413869-0-1
Com Reg Board (+/−15V)	E-UA-5413867-0-0
Com Reg Board (+/−15V)	K-PL-5413867-0-DBP
Com Reg Board (+/−15V)	D-CS-5413867-0-1
Distribution Board	D-UA-5413877-0-0
Distribution Board	K-PL-5413877-0-DBP
Distribution Board	D-CS-5413877-0-1
H7202B P.S. Eng. Spec.	A-SP-H7202-B-0
Pkg. P.S. H7202/H7200	A-SP-3700635-0-0
11730-Z Unit Assembly	E-UA-11730-Z-0
BA11-Z Unit Assembly	E-UA-BA11-Z-0

CHAPTER 2
POWER SUPPLY SPECIFICATIONS

2.1 H7202B POWER SUPPLY

Table 2-1 lists the environmental and electrical specifications for the H7202B Power Supply.

Table 2-1 H7202B Power Supply Environmental and Electrical Specifications

Parameter	Specification
Environmental Specifications	
Temperature	Operating: 5°C – 55°C (41°F – 131°F)
	Storage: –40°C – 70°C (–40F – 158°F)
Humidity	10% – 95% with maximum wet bulb of 32°C (90°F) and a minimum dew point of 2°C (36°F)
Altitude	Operating: 22.2 in Hg (8,000 feet)
	Storage: 8.9 in Hg (30,000 feet)
Cooling	External forced air cooling at 400 linear ft/min
Input Specifications	
Line Voltage/ Frequency	Low Range: 90 – 132 Vrms/47 to 63 Hz
	High Range: 180 – 264 Vrms/47 to 63 Hz
Current	8.5 A (RMS) maximum and 25 A (PEAK) maximum at a nominal line voltage of 120 Vrms
	4.2 A (RMS) maximum and 12 A (PEAK) maximum at a nominal line voltage of 240 Vrms

Table 2-1 H7202B Power Supply Environmental and Electrical Specifications (Cont)

Parameter	Specification
Inrush Current	At the first application, the stated surge current may be reached for one half the input line. Following that, there will be repetitive peaks of lower amplitude for up to 10 cycles of the line. Low Range: 120 A peak maximum High Range: 120 A peak maximum
Average Power	Average input power is 650 watts maximum when the outputs are loaded with a maximum of 400 watts.
Power Factor	The ration of real power to apparent power is greater than 0.6 at full load and nominal input voltage.
Input Line Noise Susceptibility	Low Energy Transients: Withstands a 300 V peak voltage spike* containing not more than 0.2 watt-seconds of energy per spike without causing system degradation or equipment damage. High Energy Transients: Withstands a 1 KV peak voltage spike* containing not more than 2.5 watt-seconds of energy per spike without equipment damage.
CW Noise	10 kHz – 30 mHz: 3 Vrms maximum
RF Field Susceptibility	10 kHz – 30 mHz: 1 V/M maximum 30 mHz – 1 gHz: 10 V/M maximum
Power Interruption	
Ride Through Capability	Outputs remain within limits for a minimum of 6.0 milliseconds after a low line power interruption (either voltage range).
Undervoltages	Withstands any undervoltage condition for any duration without equipment damage.
Overvoltage	Withstands an input overvoltage of 150 Vrms (low range) or 300 Vrms (high range) for one second maximum, without sustaining any equipment damage.
Output Power and Signal Characteristics	H7200 +5.1 V Power Module (Paragraph 2.1.1) H7213 Memory Power Module (Paragraph 2.1.2) H7211 Communications Power Module (Paragraph 2.1.3)

* A spike is defined as a voltage transient of either polarity and of either common or differential mode, with a rise time (10% – 90%) of 0.1 microsecond or more. The average power of spikes does not exceed 0.5 watts.

2.1.1 H7200 +5.1 V Power Module

Table 2-2 lists the internal/external dc output specifications for the H7200 +5.1 V power module.

Table 2-2 Internal/External DC Output Specifications

Internal DC Output Specifications (Used within the power supply)	Units	
BULK DC		
Nominal	Vdc	300
Maximum	Vdc	365
Minimum	Vdc	245
Ripple	V p-p	25 (at 2X line Hz)
Ripple	V p-p	5 (at 30–170 KHz)
Current	A	1.5
Internal Low Voltage (ILV)		
Nominal	Vdc	+14
Maximum	Vdc	+14.5
Minimum	Vdc	+12.5
Ripple	mV p-p	500 (at 1–170 KHz)
Current	mA	400
Nominal	Vdc	−14
Maximum	Vdc	−15
Minimum	Vdc	−12.5
Ripple	mV p-p	500 (at 1–170 KHz)
Current	mA	50
External DC Output Specifications (Used outside of the power supply)	**Units**	
Output Voltage		
Nominal	Vdc	+5.1
Overvoltage trip point	Vdc	+6.5
Maximum	Vdc	+7.0
Ripple voltage	mV p-p	100
Noise voltage	mV rms	50
Rated Current		
Maximum	Adc	60
Minimum	Adc	0
Static line/load regulation	mV dc	75
Dynamic regulation current	A	5
Over/undershoot (maximum)	mV	150
Response time (maximum)	ms	1.0
Settling time	ms	1.5
Current Limit		
Overload type	—	Pulsing
Initiation point	Adc	65–75
Short circuit (maximum)	A rms	5

Table 2-3 lists the external control signal inputs and outputs for the H7200 +5.1 V power module.

Table 2-3 External Control Signal Inputs/Outputs

External Control Signal Inputs (Inputs external to the power supply)	Function	Electrical Specifications
PWR REQ (POWER REQUEST)	Enables all outputs when pulled low externally.	
SHTDN (SHUTDOWN)	Inhibits all outputs when pulled low externally. Overrides PWR REQ and STBY signals.	Low State (Asserted) <1.6 volts; source current of −1.0 mA maximum High State (Deasserted) >100 K ohms to ground; open circuit voltage is 15 volts maximum
STBY (STANDBY)	Enables the "standby" channels (outputs) when pulled low externally. "Standby" is internally programmed to be "Channel 2" outputs (H7213 Memory Power Module).	Low State (Asserted) <1.6 volts maximum; source current of −1.0 mA maximum High State (Deasserted) >100 K ohms to ground; open circuit voltage is 1.5 volts maximum
MOD EN (MODULE ENABLE)	When asserted indicates that primary power (300Vdc) is coming from the battery backup unit (BBU). This signal shuts down the modules programmed as "nonstandby" (H7200 and H7211).	Low State (Asserted) External low impedance to power supply return, capable of sinking 3 mA minimum with a maximum voltage of 1.0 volts. High State (Deasserted) High impedance capable of blocking +15 volts with 1.0 μA maximum leakage.
AIR FLT (AIR FAULT)	Shutdown input with internal latch used with external environmental sensors. Consists of a pull-up line and fault signal which must be connected externally for normal operation.	Low State (Asserted) Low impedance to power supply return capable of sinking 10 mA with a maximum voltage of 1.0 volts.

Table 2-3 External Control Signal Inputs/Outputs (Cont)

External Control Signal Inputs (Used outside of the power supply)	Function	Electrical Specifications
AIR FLT (Cont)	When the AIR FLT line is pulled low, to power supply return, all DC power is removed after AC LOW and DC LOW are asserted. An internal latch is also set, holding this condition until PWR REQ and STBY inputs are deasserted (KEY-SWITCH set to OFF). Under default conditions with both lines open, the power supply will not operate. Minimum fault assertion time to guarantee a latch is 100 μs.	High State (Deasserted) High impedance capable of blocking +15 volts with a maximum leakage of 1.0 μA.
DC LOW	When asserted, indicates that the DC voltage at the input bus is not adequate to maintain output regulation, and that output DC power is about to drop. All outputs remain in regulation for 1.0 ms minimum after this signal is asserted. On power turn-on, this signal is asserted until regulation is reached.	Low State (Asserted) Capable of sinking 50 mA at 0.4 volts maximum. High State (Deasserted) Output impedance of 100 K ohms minimum at 15 volts maximum applied voltage.
AC LOW	When asserted, indicates that the DC voltage at the input bus is at or near the value necessary to guarantee the 5 ms hold-up time prior to DC LOW. This value is below the specified line voltage but above the minimum required for regulation. When deasserted, indicates adequate input voltage. On power turn-on, is asserted until after DC low is deasserted. On power turn-off, is asserted 5 ms minimum prior to DC LOW asserted.	Same as DC LOW.
Line Clock Signal (LTC)	Timing reference at the frequency of and synchronous with the AC line. Its waveform is a square-wave of approximately 50 percent duty cycle. Capable of driving the equivalence of 10 TTL loads. Return lead is common with DC LOW. This signal does not function when primary power (+300 Vdc) is derived from the BBU.	

Table 2-3 External Control Signals Inputs/Outputs (Cont)

External Control Signal Inputs (Inputs external to the power supply)	Function	Electrical Specifications
BAT EN (BATTERY BACK-UP ENABLE)	When asserted, assures that a valid BBU condition exists in the power supply. This enables BBU to assume the "ready" state for fast response to a powerfail condition through the BAT REQ signal. When deasserted, a non-valid condition is indicated such as thermal shutdown or DC output failure. This allows the BBU to assume the "off" state, which does not allow fast response and permits minimum battery drain in the BBU. A transition from asserted to deasserted while the BBU is supplying power, terminates the backup condition, and removes BBU power.	High State (Asserted) A voltage source of +12 volts (10.5 V minimum and 14.5 V maximum) at 10 mA maximum current. Low State (Deasserted) High impedance source of > 100 K ohms to +14.5 volts maximum.
BAT REQ (BATTERY BACK-UP REQUEST)	Momentary indication of a drop in the BULK DC power input to the power modules; indicates AC line voltage has dropped. Asserted simultaneously with AC LOW, but deasserted when the BULK DC is increased due to the input of BBU power. The minimum assertion time is $>1.0\ \mu s$.	Same as BAT EN.
BOOT EN (BOOT ENABLE)	Valid on power up between deassertion of DC LOW and AC LOW. When asserted, indicates that memory voltages have been in regulation and uninterrupted since assertion of DC LOW on the previous power down. When deasserted, indicates that memory voltages have been interrupted. Once asserted, BOOT EN stays asserted until AC LOW is deasserted.	Low State (Asserted) Capable of sinking 20 mA at 0.4 V maximum. High State (Deasserted) 180 ohms pullup to 5.1 V nominal.

2.1.2 H7213 Memory Power Module

Table 2-4 lists the output specifications for the H7213 memory power module.

Table 2-4 Output Specifications for the H7213 Memory Power Module

Parameter	Specification		
Voltage			
Nominal	Vdc	+12.3	+5.1
Overvoltage trip point	Vdc	None	+6.0
Maximum	Vdc	+15.0	+6.5
Reverse protection		YES	YES
Ripple voltage	mV p-p	200	75
Noise voltage	mV rms	100	50
Rated Current			
Maximum	Adc	3.0(*)	15.0
Minimum	Adc	0.8(**)	2.0(***)
Static line/load regulation	Vdc	600	150
Dynamic Regulation Current	A	0.6	3.0
Over/undervoltage (maximum)	mV	500	100
Response time (maximum)	ms	10	1.0
Settling time	ms	15	1.5
Current Limit			
Overload type	—	Pulsing	Pulsing
Initiation point	Adc	6.5–7.5	16–22
Short circuit	A rms	2.0	8.0

Notes to Table 2-4

* Maximum continuous output current for +12.3 V output is 3.0 A. Intermittent currents of up to 6.0 A may be drawn for several seconds if the duty cycle is keep below 2 percent. If continuous currents of greater than 3.0 A are drawn, a terminal protection switch will shut down the supply.

** The minimum load specified for the +12.3 V output is required to maintain regulation. If the minimum load is below that specified, the +12.3 V output can be out of regulation on the high side.

*** The minimum load specified for the +5.1 VB output is required to maintain regulation on the −12.3 V output. The +5.1 VB output will operate at no load, but the +12.3 V output will be below specification.

2.1.3 H7211 Communications Power Module

Table 2-5 lists the output specifications for the H7211 communications power module.

Table 2-5 Output Specifications for the H7211 Communications Power Module

Parameter	Specification		
Voltage			
Nominal	Vdc	+15.0	−15.0
Overvoltage trip point	Vdc	17-19.1	16.7–18.8
Maximum	Vdc	+21.0	−21.0
Reverse protection		NO	YES
Noise	mV p-p	150	150
Ripple	mV rms	200	300
Rated Current			
Maximum	Adc	2.0	3.0
Minimum	Adc	0	0
Static line/load regulation	mV dc	100	150
Dynamic Regulation Current	A	.2	.3
Over/undervoltage (maximum)	mV	200	50
Settling time	ms	0.5	250
Current Limit			
Overload type	—	Foldback	Foldback
Initiation point	Adc	2.1–2.6	3.1–3.7
Short circuit	Adc	0.5	1.5

2.2 OPERATING INSTRUCTIONS

To enable the H7202B Power Supply:

1. Make sure the six-position KEYSWITCH on the VAX-11/730 front panel is set to the OFF position.
2. Set the power supply line voltage select switch S1 to the appropriate line voltage setting (120 Vac or 240 Vac).
3. If the battery backup unit is optioned, set the voltage select switches to the appropriate line voltage setting.
4. Set the AC Power Controller FUNCTION switch to LOCAL.
5. Set the power supply circuit breaker CB1 to ON.
6. Set the KEYSWITCH to the desired position.

To disable the H7202B Power Supply:

1. Set the KEYSWITCH to the OFF position.
2. Set the power supply circuit breaker to OFF.

CHAPTER 3
MECHANICAL CONFIGURATION AND POWER/SIGNAL DISTRIBUTION

3.1 MECHANICAL CONFIGURATION

The location of the H7202B Power Supply within the BA11-Z mounting box of the VAX-11/730 system cabinet assembly is illustrated in Figure 3-1. It is mechanically and electrically configured as follows (refer to Figures 3-2 and 3-3):

- The ac power assembly (excluding the ac line filter) is mounted in the top front of the power supply box assembly.

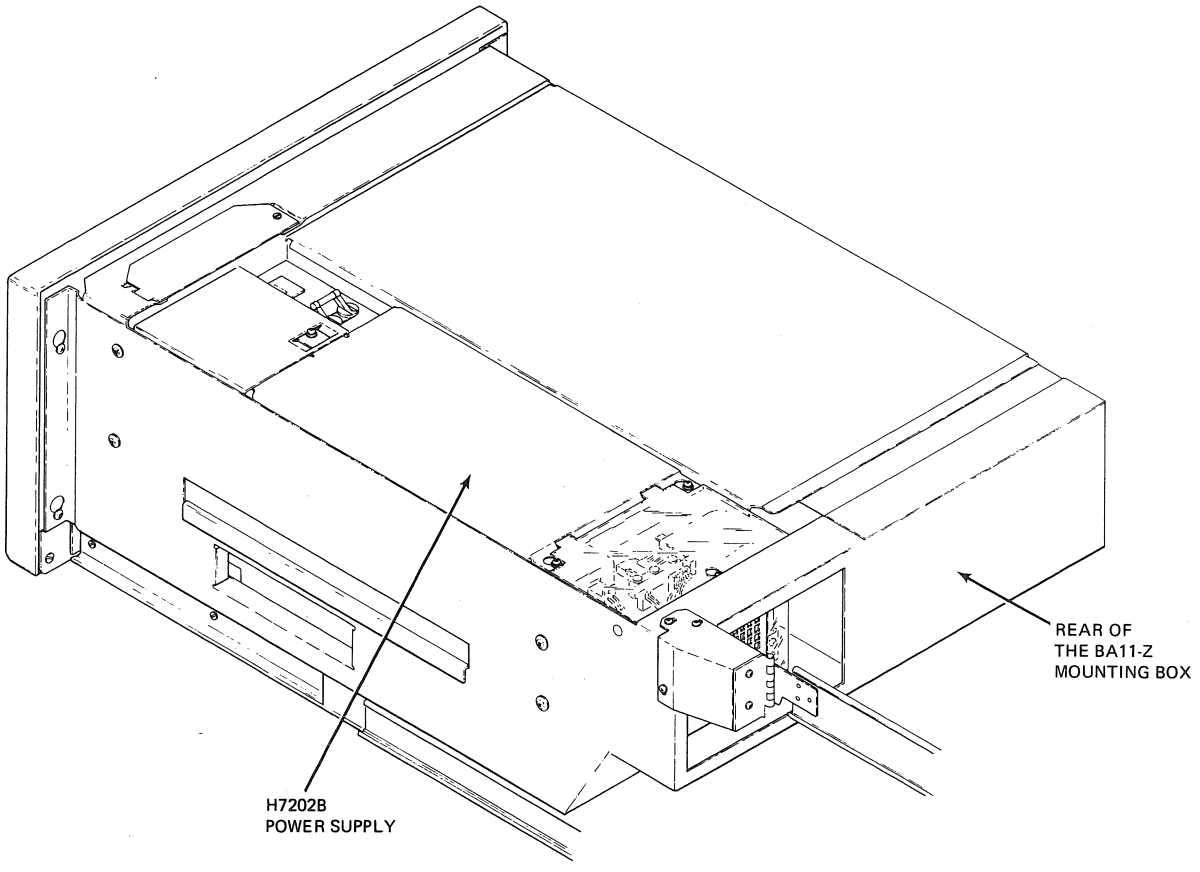


Figure 3-1 H7202B Power Supply Location Within the BA11-Z Mounting Box of the VAX-11/730 System Cabinet Assembly

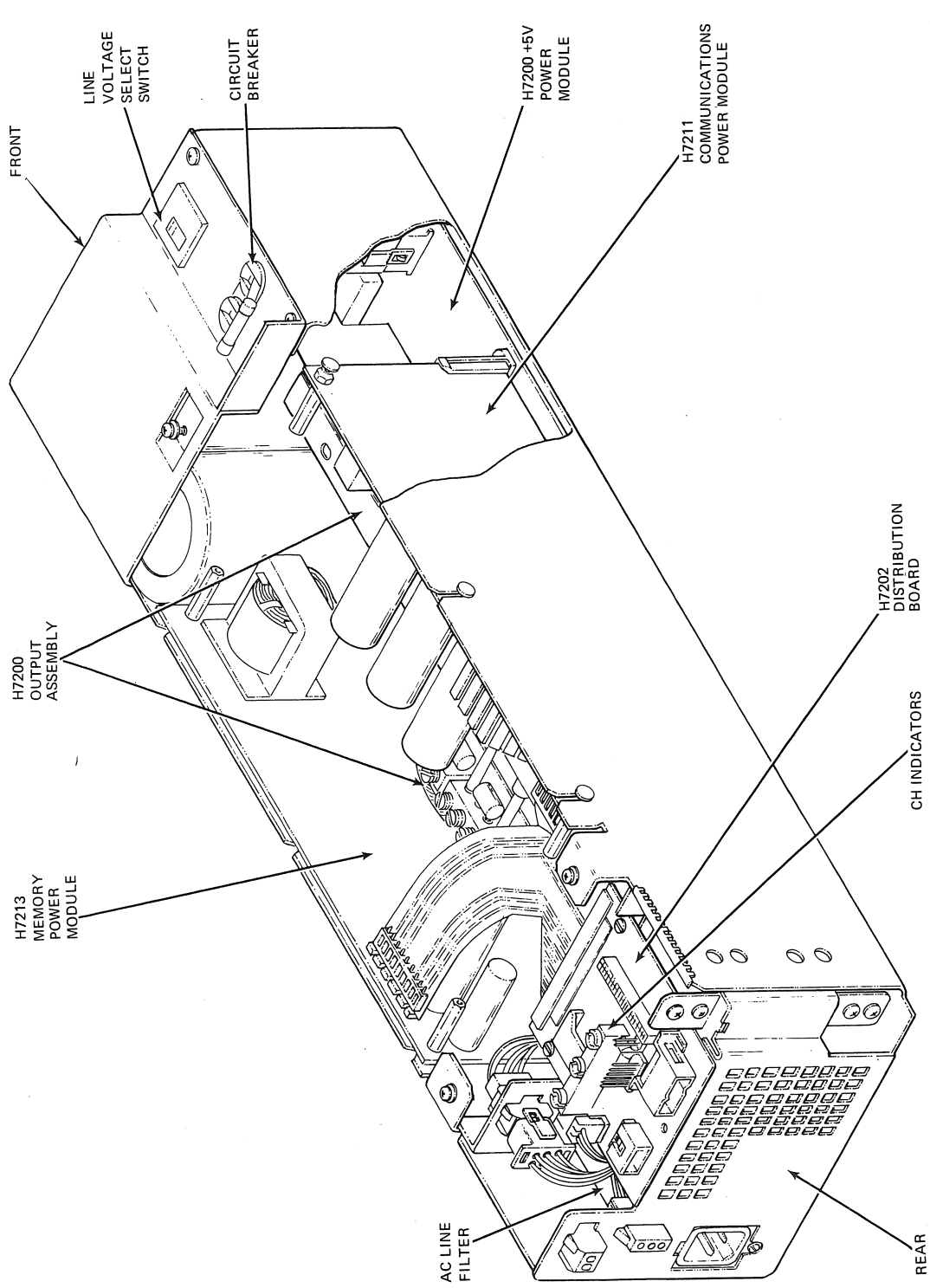


Figure 3-2 Mechanical Configuration of the H7202B Power Supply

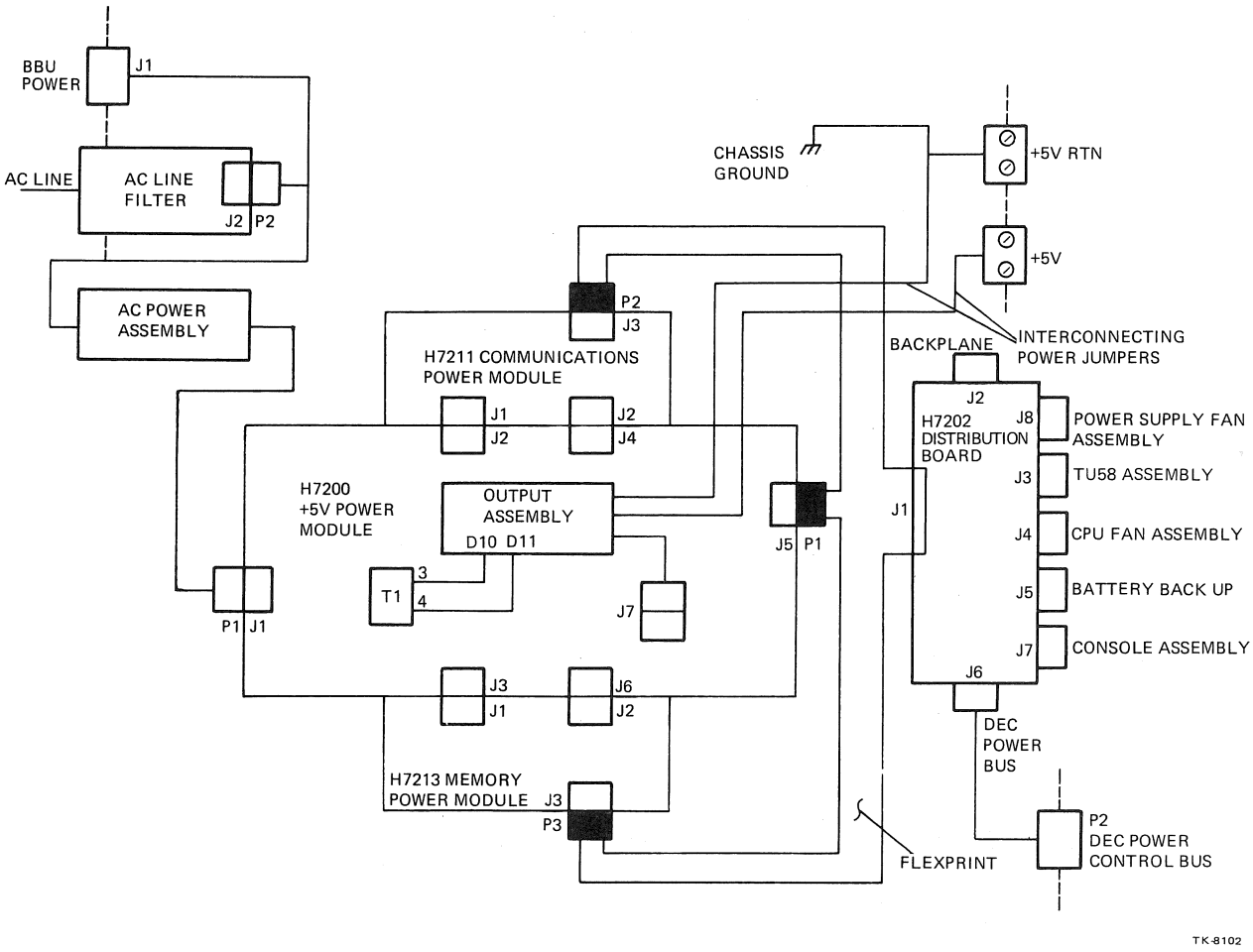


Figure 3-3 Electrical Configuration of the H7202B Power Supply

- The H7200 is mounted in the bottom of box assembly with the output assembly mounted onto it. The output assembly is connected to it by cables from TI-3 and T1-4 and a four wire harness to J7. The H7200 is connected to the ac power assembly through J1 (located in the left front corner of the H7200) to P1 (from the ac power assembly).

- The ac line filter is mounted to the rear right of the power supply box assembly. It is connected to the ac input assembly through a six wire harness (from the ac input assembly) which is routed underneath the H7200 to the connector mounting bracket at the rear of the box assembly where P2 is connected to J2.

- The H7213 is mounted vertically at the right side of the box assembly to the H7200 by connecting J1 and J2 to J3 and J6, respectively.

- The H7211 is mounted vertically at the left side of the box assembly to the H7200 by connecting J1 and J2 to J2 and J4, respectively.

- The H7202 distribution board is mounted to the top rear of the box assembly. It is interfaced to the H7200, H7213, and H7211 through the flexprint to connectors J5, J3, and J3, respectively.

3.2 H7202B POWER SUPPLY REMOVAL AND REPLACEMENT

To remove and replace the H7202B Power Supply from the mounting box (refer to Figure 3-4):

NOTE

The H7211 and H7213 power modules can be replaced without removing the H7202B power supply from the BA11-Z mounting box.

1. Make sure the power supply circuit breaker is set to OFF.
2. Loosen the distribution board cover holding a phillips head screw and remove it.
3. Disconnect the following cables from the rear of the power supply:
   a. The AC line power cord.
   b. Remove the four slotted head screws and the two main power flexprints from the power output connectors.
   c. The BBU power cable (if connected).
   d. The DEC POWER CONTROL BUS cable.
   e. The CPU power/signal flexprint from J2 on the distribution board.
   f. The TU58 power cable from J3 on the distribution board.
   g. The BBU signal cable from J6 on the distribution board (if connected).
   h. The console signal cable from J7 on the distribution board.
   i. The CPU fan power/signal cable from J4 on the distribution board.
   j. The power supply fan power cable from J8 on the distribution board.
4. Remove the phillips head screw at the rear of the power supply holding the two ground wires.
5. Remove the four power supply mounting screws on the right side of the BA11-Z mounting box.
6. Remove the front fan access cover and loosen the phillips head screw to the left of the fan.
7. Loosen the rear power supply hold down clamp and slide it back.
8. Slide the power supply back out of the front hold down clamp and lift it (by the front) out of the top of the mounting box.

To replace the H7202B Power Supply, reverse the removal steps.

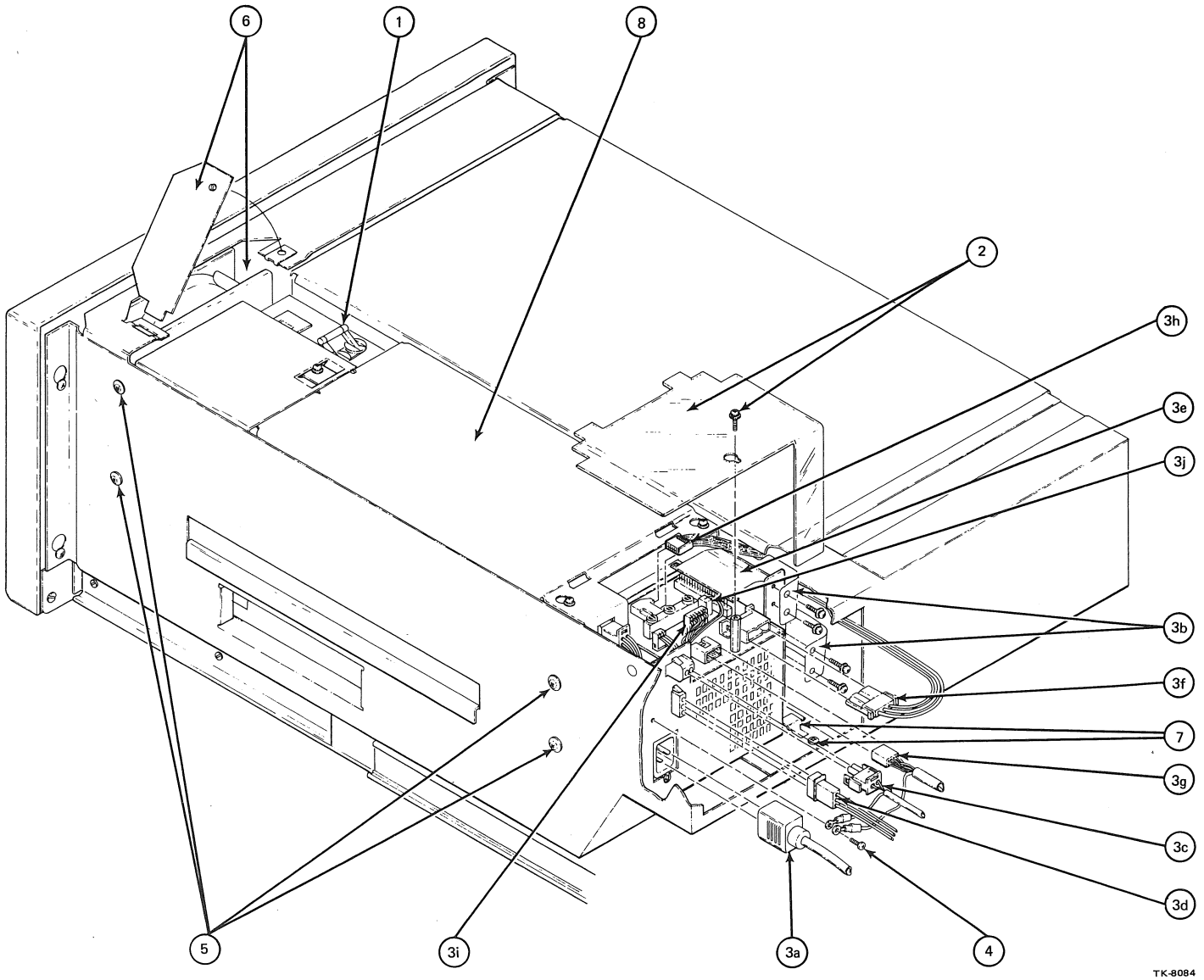


Figure 3-4 Power Supply Removal from the BA11-Z Mounting Box

3.3 H7202B POWER SUPPLY DISASSEMBLY AND ASSEMBLY

To disassemble the power supply (refer to Figure 3-5):

1. Loosen the three phillips head screws on the distribution board cover and remove it.
2. Disconnect ac connector P2 from J2 on the connector mounting bracket at the rear of the supply, which locks the module cover down.
3. Loosen the module cover front (one) and rear (two) hold down phillips head screws and remove the cover.
4. Disconnect the flexprints from the H7211 and H7213 power modules.

NOTE
DO NOT make any sharp bends in the flexprints when you disconnect them.

5. Grasp the module handles (standoffs) on the H7211 and H7213 and pull the modules straight up and out of the power supply.

NOTE
Remove the power modules by pulling on the module handles ONLY.

6. Remove the four phillips head screws on the ac power assembly, then disconnect the cable leading from it to the H7200 and remove the assembly.
7. Disconnect the flexprint from the H7200 power module.
8. Remove the four phillips head screws holding the power output jumpers to the H7200 output assembly.
9. Remove the six philips head H7200 mounting screws from the bottom of the power supply.
10. Grasp the H7200 output assembly and slide the H7200 power module out of the front of the power supply.

To assemble the power supply, reverse the disassembly steps plus:

1. When inserting the H7211 and H7213 power modules, make sure they slide into the module guides.
2. When connecting the power output jumpers to the H7200 output assembly, torque the screws to 16 IN-LBS.

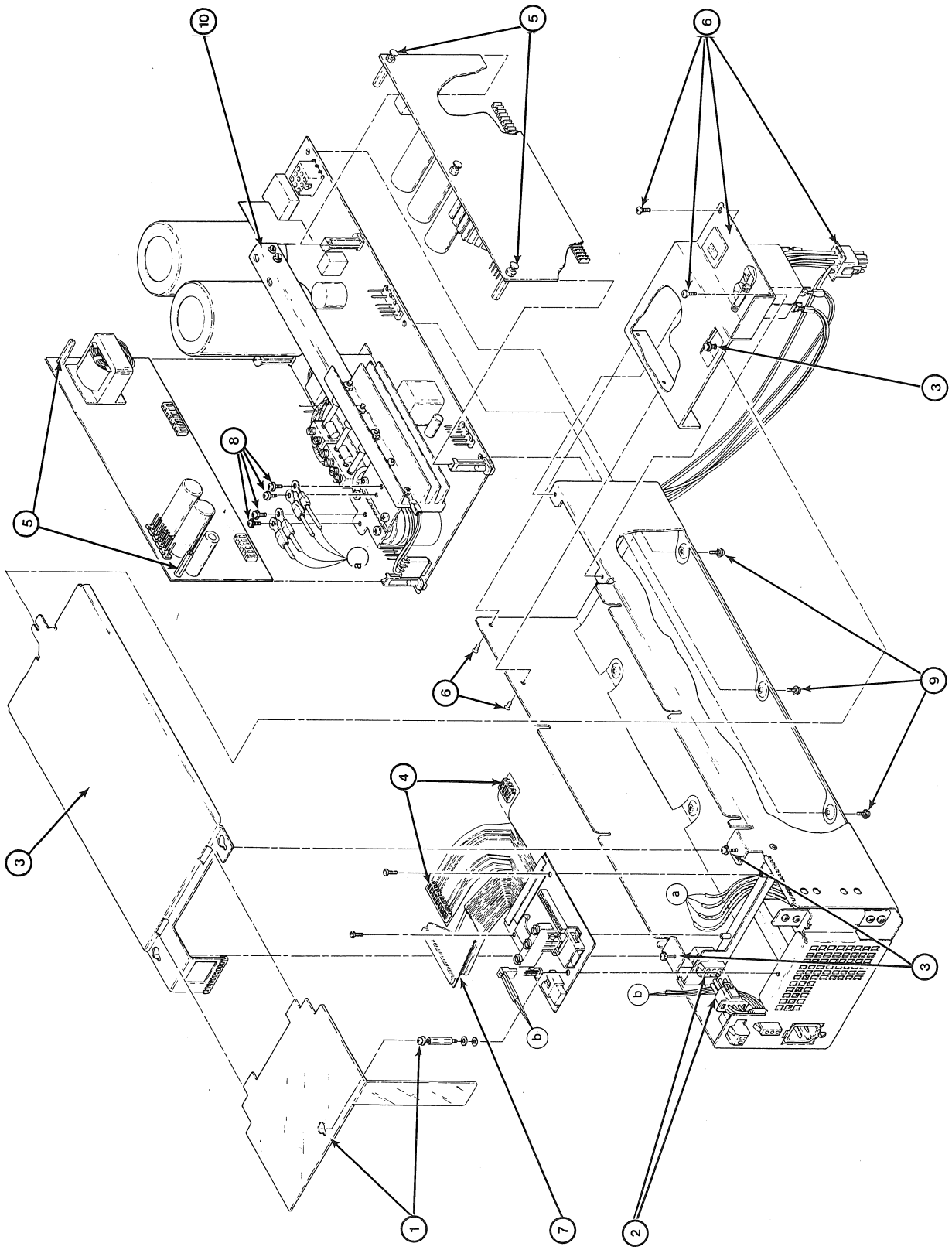


Figure 3-5 H7202B Power Supply Disassembly

3.4 POWER DISTRIBUTION

Power distribution outside the H7202B power supply is illustrated in Figure 3-6.

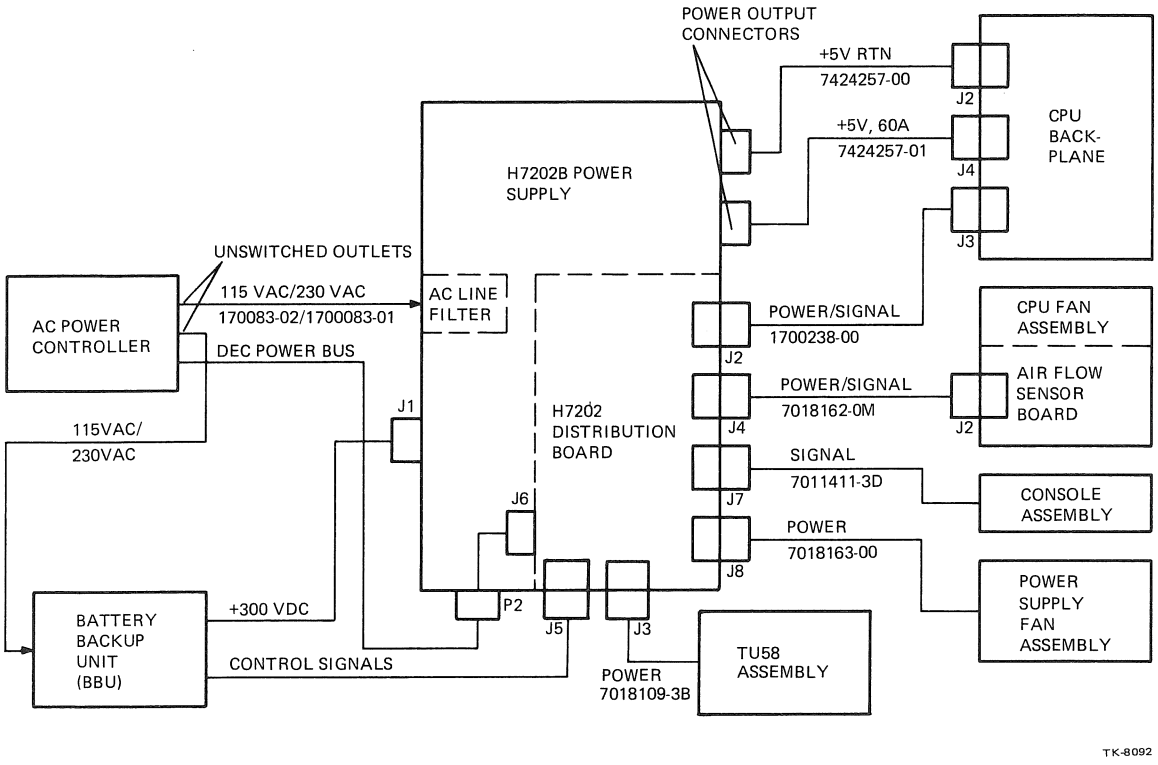


Figure 3-6 Power/Signal Distribution Outside the H7202B Power Supply

3.4.1 Ac Power Distribution

Ac line power is routed from the unswitched outlets on the ac power controller through the ac line cord (1700083-02 for 115 VAC and 1700083-01 for 230 Vac) into the power supply and to the line filter. Ac input power is distributed from the line filter to the ac power assembly through P2 and J2 respectively. Input power from the ac power assembly is routed to the H7200 through connectors J1 and P1 respectively.

If the optional BBU is installed, ac power is also routed from the unswitched outlets on the ac power controller into the BBU.

3.4.2 Dc Power Distribution

3.4.2.1 Dc Power Distribution in the Power Supply – The H7213 and H7211 receive ILV (+/−14 volts) and bulk dc (+/−150 volts) from the H7200 through J1 to J3 and J1 to J3, respectively.

3.4.2.2 Dc Power Distribution Outside the Power Supply – All dc voltages (except +5 V, 60 A and +300 V BBU) are routed from the power modules (J5 on the H7200, J3 on the H7211, and J3 on the H7213) through the flexible distribution circuit (17000213-00) to the H7202 distribution board (refer to engineering drawings CS-5413877-0-1 and IC-H7202-0-2) where they are distributed outside the power supply.

Table 3-1 lists the voltages on the distribution board, source connectors, destinations, and part number of the cable harness these voltages are routed through. Figure 3-7 illustrates the output connectors on the power supply.

Table 3-1 Dc Distribution Outside the H7202B Power Supply

Voltage	Source	Cable Harness	Destination
+5 VB, +15 V and −15 V	Distribution Board J2	1700238-00	CPU Backplane J3
+12.3 V	Distribution Board J8	7018163-00	Power Supply Fan
+5 V and +12.3 V	Distribution Board J4	7018162-00	CPU Fan Flow Sensor J2
+5 VB and +12.3 V	Distribution Board J3	7018109-3B	TU58 Assembly
TOY +5 V	BBU		Distribution Board J5

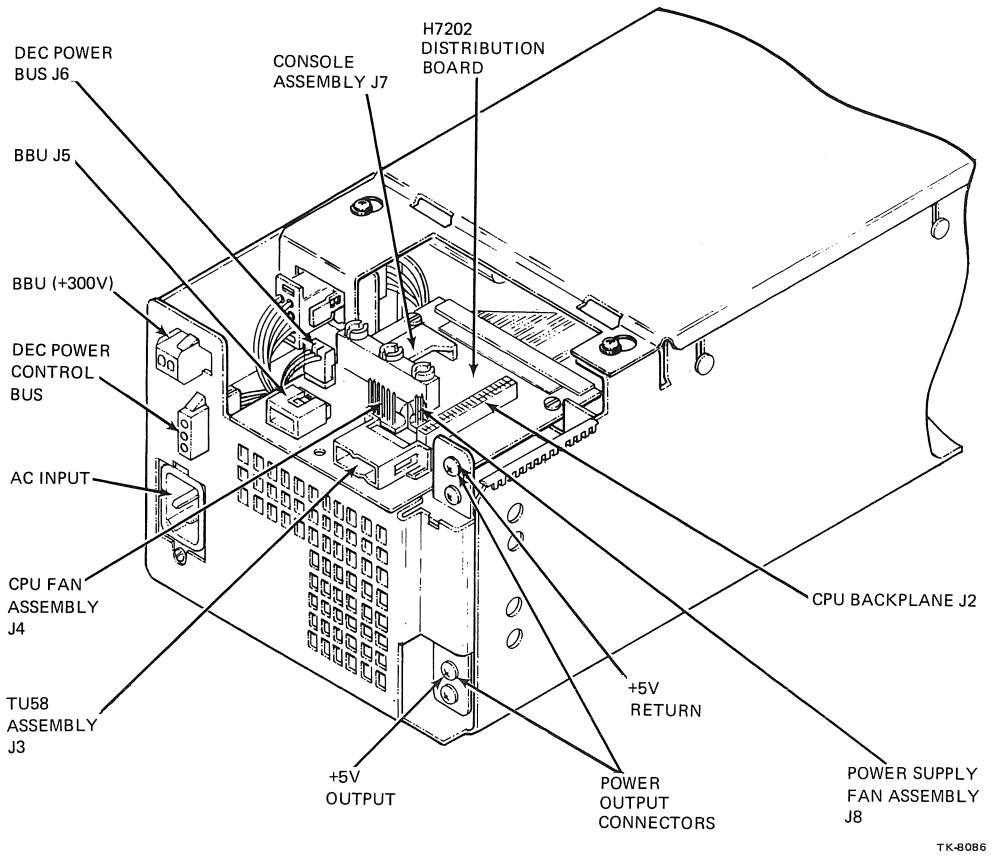


Figure 3-7 Input/Output Connectors on the H7202B Power Supply

3.4.2.3 Dc Power to the CPU Backplane – The +5 V, 60 A output is routed from the output assembly through interconnecting power jumpers (two for the +5 V terminal; two for the RTN terminal) to the power output connectors (7424257-00 for RTN; 7424257-01 for +5V) located at the left rear of the power supply. The output is then routed from the power output connectors through two power flexprints (1700239-00) to the CPU backplane (the +5 V cable is routed to J4; the RTN cable is routed to J2).

NOTE

When the BBU is not installed, the +5 volts for the time of year clock (TOY) is taken from the power supply. The +5 volts is jumpered from J5-1 to J5-2 on the BBU connector located on the distribution board. This voltage is then routed to the CPU through connector J2 on the distribution board. However, when the BBU is installed, the BBU supplies the +5 volts TOY power through J5 (see Table 3-1.).

3.4.2.4 Dc Power from the BBU – The +300 Vdc power from the BBU is connected to the rear of the power supply at J1. This battery backup power is routed through the ac power assembly (P2 to J2) into the H7200 (J1 and P1).

3.5 CONTROL SIGNAL DISTRIBUTION

Engineering drawing IC-H7202-0-2 illustrates signal distribution in the H7202B power supply. Figure 3-6 illustrates signal distribution outside the H7202B power supply (see also engineering drawing IC-H7202-0-2).

All power supply control signals are routed from J5 on the H7200 through the flexprint (1700213-00) to the H7202 distribution board (refer to engineering drawing CS-5413877-0-0) where they are distributed outside the power supply (except for PWR REQ and SHTDN, see NOTE).

NOTE

The control signals from the ac power controller (PWR REQ and SHTDN) are connected to the rear of the power supply at the DEC POWER CONTROL BUS connector, then routed to J6 on the distribution board.

Table 3-2 lists the control signals used in the power supply, sources, destinations, and part numbers of the cable harnesses these signals are routed through. Refer to Figure 3-7 for location of the input/output connectors on the power supply.

Table 3-2 Control Signal Distribution for the H7202B Power Supply

Signal	Source	Cable Harness	Destination
+/–SENSE	Backplane J3	1700239-00	Distribution Board J2
AIR FLT	CPU Air Flow Sensor J2	7018162-00	Distribution Board J4
MOD EN	BBU		Distribution Board J5
SHTDN	Ac Power Controller		Distribution Board J6
PWR REQ	Console	7011411-3D	Distribution Board J7
STBY	Console	7011411-3D	Distribution Board J7
AC LO	Distribution Board J2	1700238-00	CPU Backplane J3
DC LO	Distribution Board J2	1700238-00	CPU Backplane J3
LTC	Distribution Board J2	1700238-00	CPU Backplane J3
BOOT EN	Distribution Board J2	1700238-00	CPU Backplane J3
BAT EN	Distribution Board J5		BBU
BAT REQ	Distribution Board J5		BBU
FAULT PULL-UP	Distribution Board J4	7018162-0M	CPU Air Flow Sensor J2

CHAPTER 4
FUNCTIONAL DESCRIPTION

The H7202B power supply is the source of power for the VAX-11/730. The power supply (Figure 4-1) is composed of the ac input power assembly, +5.1 V power module (H7200), the memory power module (H7213) and the communications power module (H7211).

The ac input power assembly controls the application of ac line voltage to the +5.1 V power module.

The +5.1 V power module accepts the ac line voltage to generate the power supply BULK DC and regulated internal low voltage (ILV) and the regulated +5.1 V, 60 A, output for the CPU backplane and CPU fan assembly. Also generated here are the power supply control, master clock, and status signals.

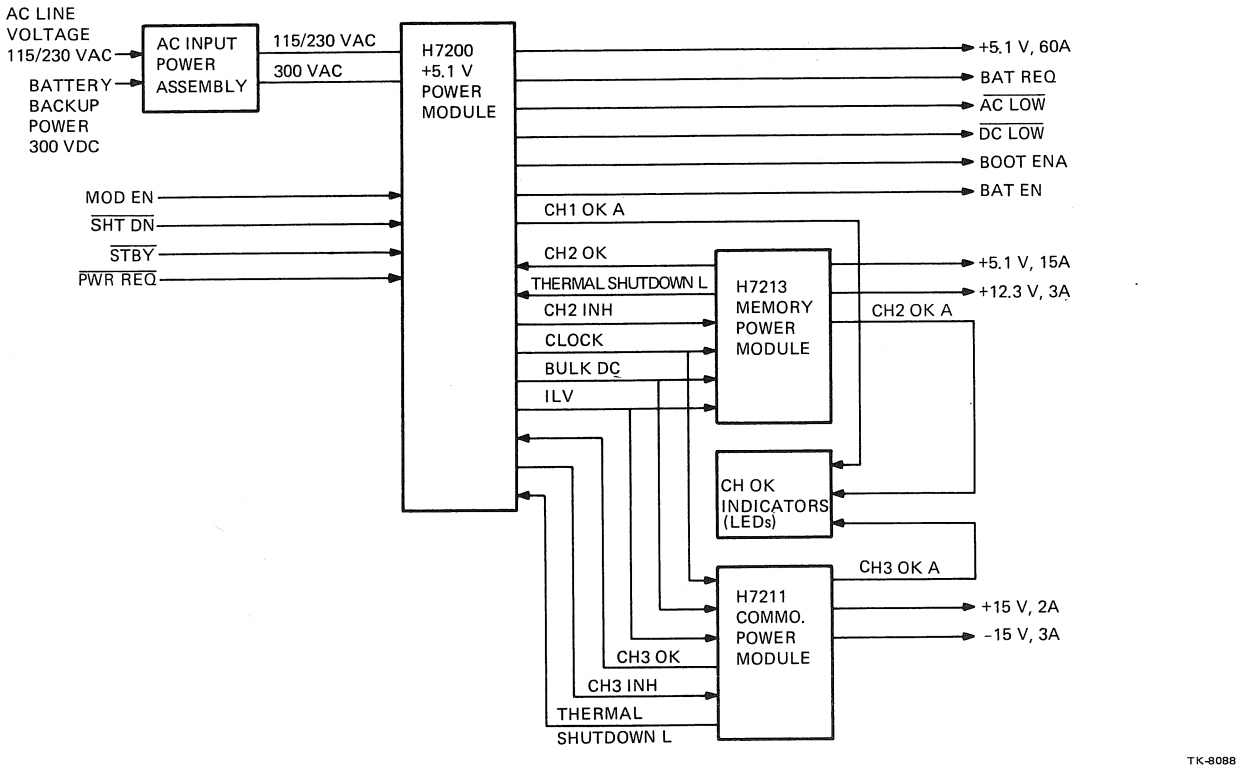


Figure 4-1 The H7202B Power Supply Block Diagram

The memory power module accepts the BULK DC, ILV, and clock signal from the +5.1 V power module to generate and regulate the +12.3 V, 3 A, output for the TU58 and power supply cooling fans and the +5 VB, 15 A, output for the TU58 and memory modules in the CPU backplane. (The B associated with the +5.1 VB indicates this voltage is a output voltage of the H7213 and not the H7200.)

When the BBU is installed, its 300 V output is used, in place of the BULK DC, by the memory power module to maintain the + 5 VB and +12.3 V outputs for a minimum of 10 minutes following a power down condition which resulted from a loss of the ac input line voltage.

The communication power module accepts the BULK DC, ILV, and clock signal from the +5.1 V power module to generate the regulated +15 V, 2 A, and −15 V, 3 A, outputs for communications modules in the backplane.

NOTE

In this chapter CH 1 refers to the H7200, CH 2 refers to the H7213, and CH 3 refers to the H7211. Voltages used in this description are approximate.

4.1 AC INPUT POWER ASSEMBLY

The ac input power assembly (Figure 4-2) contains the input ac line voltage filter, and the power supply line voltage select switch and circuit breaker. Also, the battery backup power (300 Vdc) is routed through this assembly.

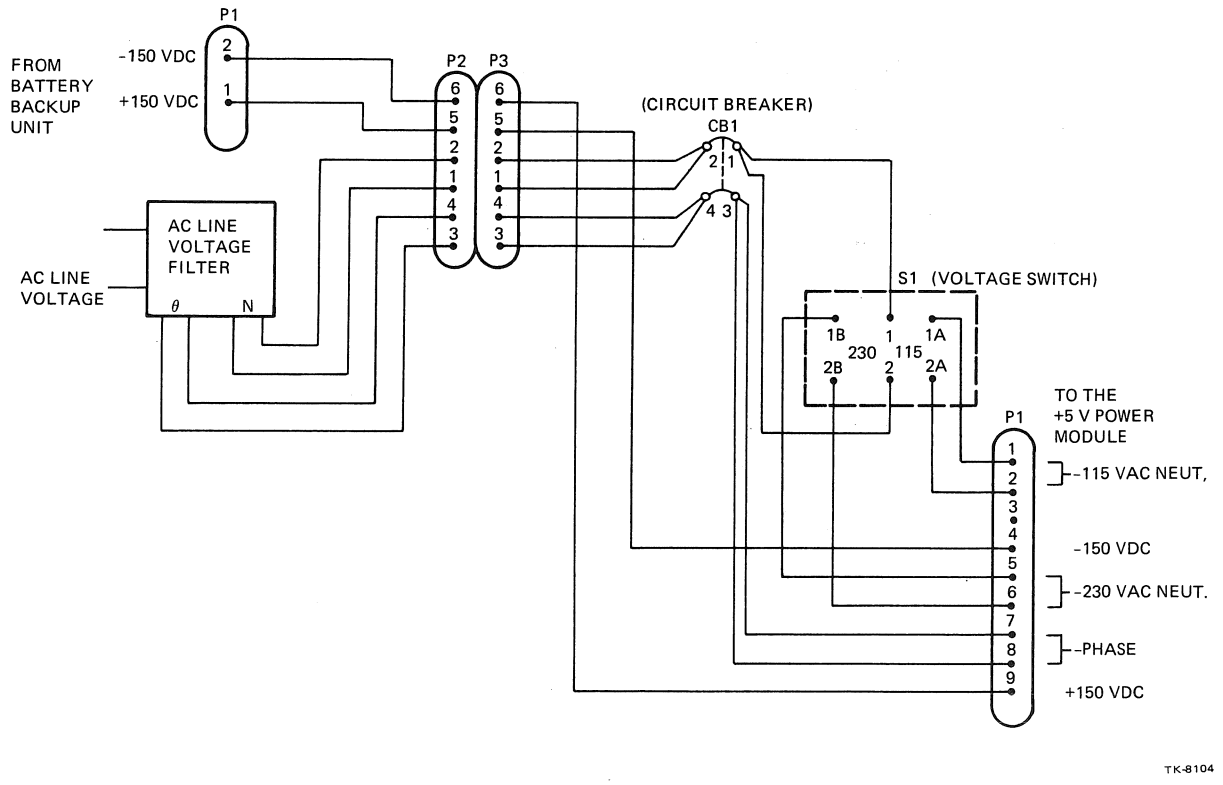


Figure 4-2 The AC Input Power Assembly (7018136-00) Wiring Diagram

The ac line voltage is routed from the ac line voltage filter through P2 and P3 (pins 1, 2, 3, and 4) to circuit breaker CB1. When CB1 is set to ON and the voltage switch (S1) is set to the approprate input ac line voltage (either 115 Vac or 230 Vac), that voltage is applied to the +5.1 V power module through P1 (115 Vac pins 1,2,7, and 8 or 230 Vac pins 5,6,7, and 8).

If the optional BBU is installed and enabled for operation (refer to Paragraph 4.2.4.2) the battery back up power (300 Vdc) is applied to J1 (pins 1 and 2) and routed through P1 (pins 4 and 9) to the +5.1 V power module.

4.2 H7200, +5.1 V POWER MODULE

The +5.1 V power module (Figure 4-3) contains the BULK DC, ILV, and +5.1 V 60 A, power supplies and the power supply control and status reporting circuit.

4.2.1 BULK DC Power Supply

The BULK DC power supply accepts the ac line voltage to generate the +/−150 Vdc BULK DC. Also, the battery backup power is routed through this supply to directly supply voltage to it during line outages. The following description is keyed to Figure 4-4 and engineering drawing 5413857.

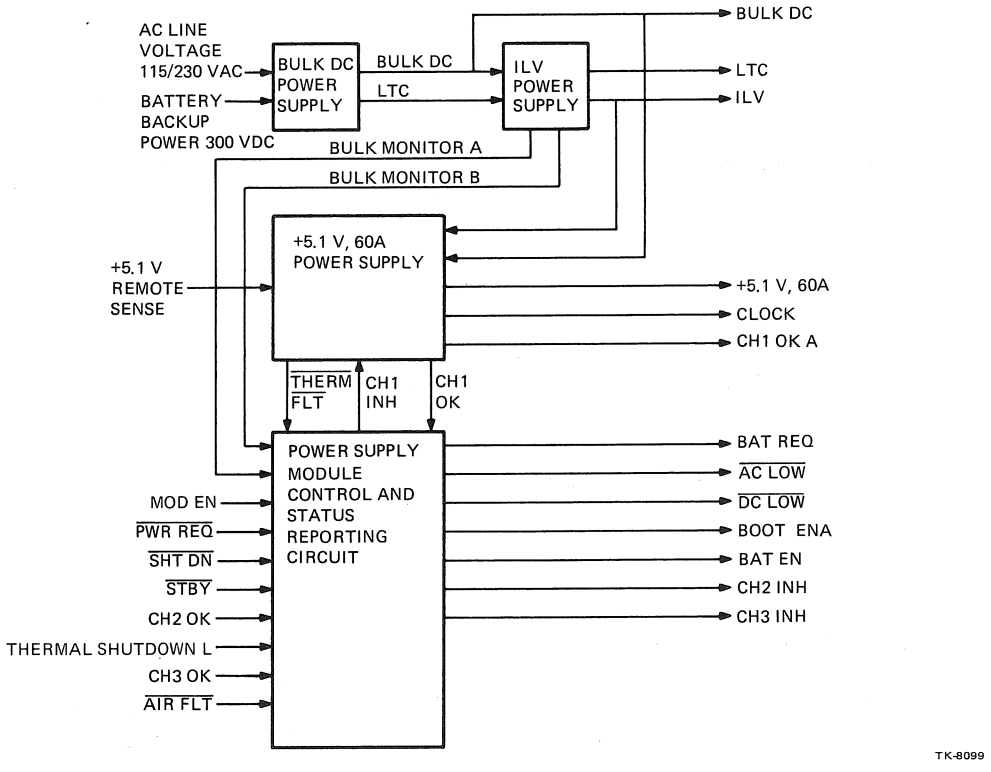


Figure 4-3 The H7200 +5.1 V Power Module Block Diagram

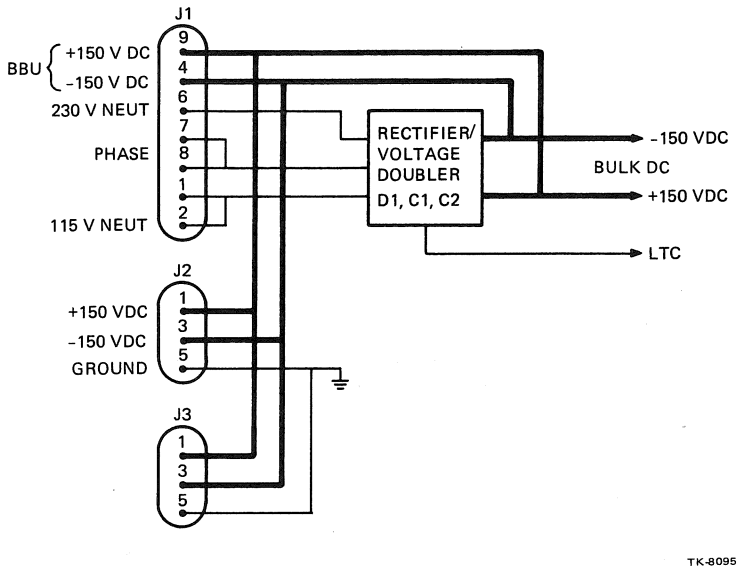


Figure 4-4 The BULK DC Power Supply Block Diagram

When the power supply circuit breaker (CB1) is set to ON, the ac line voltages are applied to J1 (pins 1,2,7, and 8 for 115 Vac or pins 6,7, and 8 for 230 Vac). This voltage is routed through surge current limiting thermistors (R1 and R2) to the rectifier/voltage doubler (D1, C1 and C2). This supply then operates as either a voltage doubler when 115 Vac is used as the input line voltage or as a bridge rectifier and filter when 230 Vac is used as the input line voltage to produce the BULK DC of +150 Vdc and -150 Vdc (300 Vdc). Also, the phase input (J1-8 and J1-7) of the ac input voltage is used to generate the line time clock signal (LTC).

NOTE
The BULK DC varies with the ac line voltage for a total of 300 Vdc (245-365 Vdc).

The BULK DC is applied to the internal low voltage supply and the +5.1 V power supply. This voltage is applied to the communications power module (through J2-1 and J2-3), and the memory power module (through J3-1 and J3-3).

4.2.2 Internal Low Voltage (ILV) Power Supply

The ILV power supply accepts the BULK DC or battery backup voltage (if the optioned BBU is installed and enabled) to generate and regulate the +14 V and -14 V ILVs. Also generated here are BULK MONITOR A, BULK MONITOR B, and LTC. The following descriptions are keyed to Figure 4-5 and engineering drawing CS-5413857.

4.2.2.1 ILV Generation and Regulation – The ILV power supply generates the +14 V and -14 V by a 33 KHz pulse width modulated flyback technique. These outputs are then regulated by the voltage produced on secondary winding (pins 3 and 4) of transformer T4. These voltages are only used within the power supply.

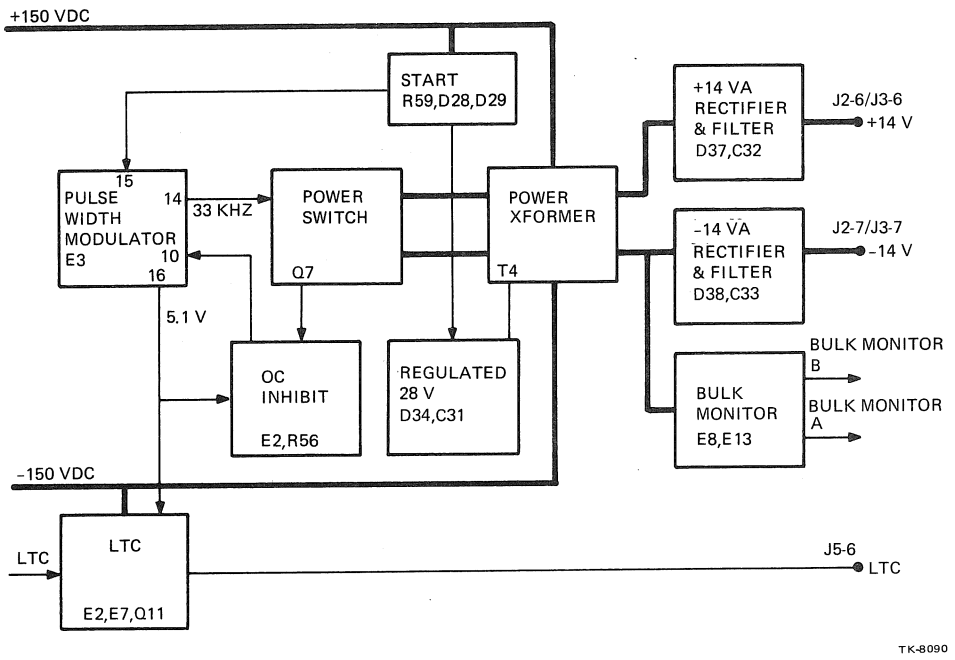


Figure 4-5 The Internal Low Voltage Power Supply Block Diagram

When the BULK DC is applied, C31 charges through R59, to 28 volts. At 28 volts, D28 conducts switching D29 on. D29 connects the 28 volts, (now the control voltage) to pin 15 of the master pulse width modulator (E3, see Appendix A). Its ramp generator produces a 66 KHz sawtooth (pin 5) which, together with the +5.1 V internal reference (pin 2) and the control voltage (pin 1), produces 33 KHz pulses at pin 14. The soft start circuit (internal to E3, controlled by C52) ensures these pulses start at 0 % of the duty cycle and gradually increases in pulse width to a maximum of 50 % duty cycle.

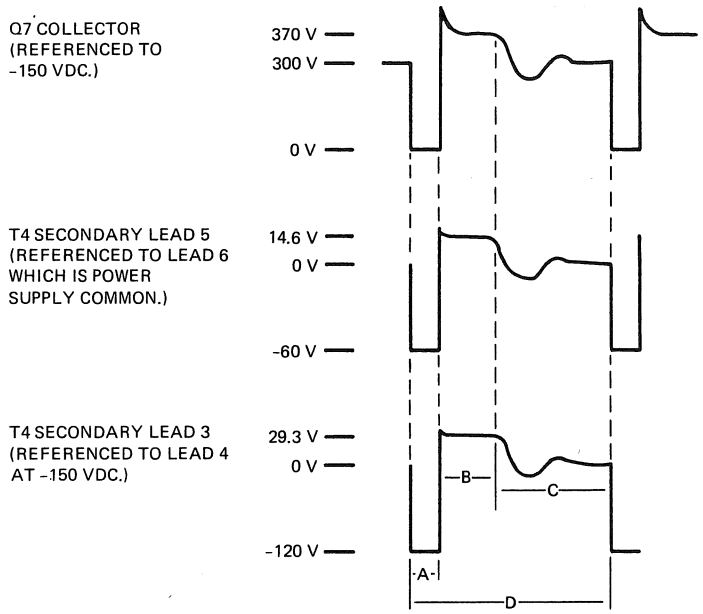
The 33 KHz pulses of E3 biases the power switch (Q7) on and off before C31 is completely discharged, (since it is suppling power for E3) to generate the +14 V and −14 V ILVs. When the voltage level of the pulse (E3-14) goes high, Q7 is biased on, dropping the BULK DC across the primary (pins 1 and 2) of the power transformer (T4). Voltage induced on the secondary (pins 3 and 4) biases D34, D37, and D38 off. As the voltage level of the pulse goes low, Q7 is biased off and the BULK DC is removed from T4.

Energy stored in the primary of T4 is now delivered to the secondaries. This voltage biases D34, D37, and D38 on (Figure 4-6). Positive secondary voltage is rectified and filtered by D37, C32, and C34 to become the +14 V internal low voltage. Negative secondary voltage is rectified and filtered by D38, C33, and C35 to become the −14 V ILV. D34 and C31 correct and filter the 28 volts at the control secondary (pins 3 and 4) of T4, to power E3. E3 then regulates the 28 volt level, by increasing or decreasing its pulse width, to regulate the +14 V and −14 V ILVs.

The ILVs are applied to the +5.1 V power supply, the power supply module control and status reporting circuit, and the memory and communications power modules. ILVs are applied to these other power modules at J2-6/J3-6 (+14 V) and J2-7/J3-7 (−14 V).

NOTE

The voltage level of ILVs is referenced to the power supply common on the schematic.



NOTES
- A) Q7 ON, ENERGY STORED IN T4, TIME INCREASES AS LOAD INCREASES (OR LINE DECREASES).
- B) ENERGY DELIVERED TO SECONDARIES OF T4 (5-6, 6-7 AND 3-4), TIME INCREASES AS LOAD INCREASES.
- C) DEAD TIME, TIME DECREASES AS LOAD INCREASES.
- D) ONE CYCLE AT 30 μS NOMINAL.

TK-8098

Figure 4-6 Waveforms of the Power Switch Q7 Output Compared to the Power Transformer T4 Output

4.2.2.2 ILV Power Supply Overcurrent Protection – Overcurrent protection in the ILV power supply is provided by the overcurrent inhibit circuit.

If an overcurrent condition occurs, the circuit inhibits the operation of the supply. If either output of the supply is overloaded, current increases through the primary power transformer (T4) when the power switch (Q7) is biased on. Comparator E2 senses this increase as an increase in voltage across resistor R65.

E2 compares this voltage with a scaled down reference voltage to produce a high (pin 1) at pin 10 of the master pulse width modulator (E3) terminating the pulse from pin 14, shutting off Q7. Early pulse termination due to overcurrent causes the ILV outputs to decrease. This continues until the overcurrent no longer exists.

4.2.2.3 BULK MONITOR A and BULK MONITOR B Generation – The BULK MONITOR A and BULK MONITOR B signals indicate the level of the +150 and –150 Vdc lines (BULK DC) to the power supply control and status reporting circuit.

When the ILV supply is producing the internal low voltages, BULK MONITOR A and BULK MONITOR B are operational. When the power switch (Q7) is biased on, pin 7 of the power transformer (T4) is high. This biases D39 on, charging C36 to one fifth of the BULK DC voltage applied to the primary (T4-1 and T4-2) of T4. (This is due to a five-to-one turns ratio between T4-1, T4-2 and T4-6, T4-7.)

The voltage on C36 is divided by R80 and R81, and buffered by E8-8, E8-9, and E8-10. Two comparators (E13) monitor this voltage to indicate the level of BULK DC. If the BULK DC drops below 200 volts, the buffered voltage drops causing BULK MONITOR A (E13-13) to go low. Should the BULK DC drop lower (below 175 volts), the buffered voltage drops lower causing BULK MONITOR B (E13-14) to go low. R83 and R85 provide hysteresis for the comparators.

4.2.2.4 LTC Generation – The LTC signal is a timimg reference for the CPU, which is at the frequency of and synchronous with the ac line voltage.

NOTE

This signal is not present during the battery backup mode.

When the ILV power supply is producing the internal low voltages, LTC is generated. When the ILV power supply master pulse width modulator (E3) is enabled, the internal reference (pin 16) is compared to LTC (ac phase) from the BULK DC power supply E2-6 and E2-5. E1 drives Q11 to produce a squire wave output at J5-6 (Figure 4-7). The duty cycle of this output varies with the variations in line voltage.

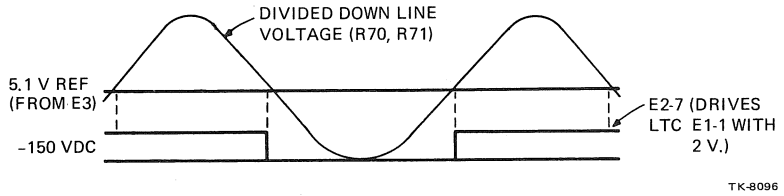


Figure 4-7 LTC Development from AC Phase and E3's 5.1 Volt Reference

4.2.3 +5.1 V Power Supply

The +5.1 V power supply accepts the BULK DC to generate and regulate the +5.1 V, 60 A, output. The following description is keyed to Figure 4-8 and engineering drawing CS-5413857-0-1.

4.2.3.1 +5.1 V, 60 A Generation – The +5.1 V, 60 A output is derived from the BULK DC by a half wave pulse width modulated forward converter operating at 33 KHz. The control circuit of this converter is the 3527A (E6, see Appendix A). This supply has undervoltage, overvoltage, and overcurrent sensing circuitry which are controlled by a 3543 (E4) (see Appendix B).

The +5.1 V power supply generates the + 5 V output when the CH1 INH signal (from the power supply control status reporting circuit) is deasserted (low).

NOTE

The default condition of CH1 INH is high, which inhibits E6 through shutdown pin 10, preventing operation of the 5.1 volt output leaving pins 11 and 14 of E6 high.

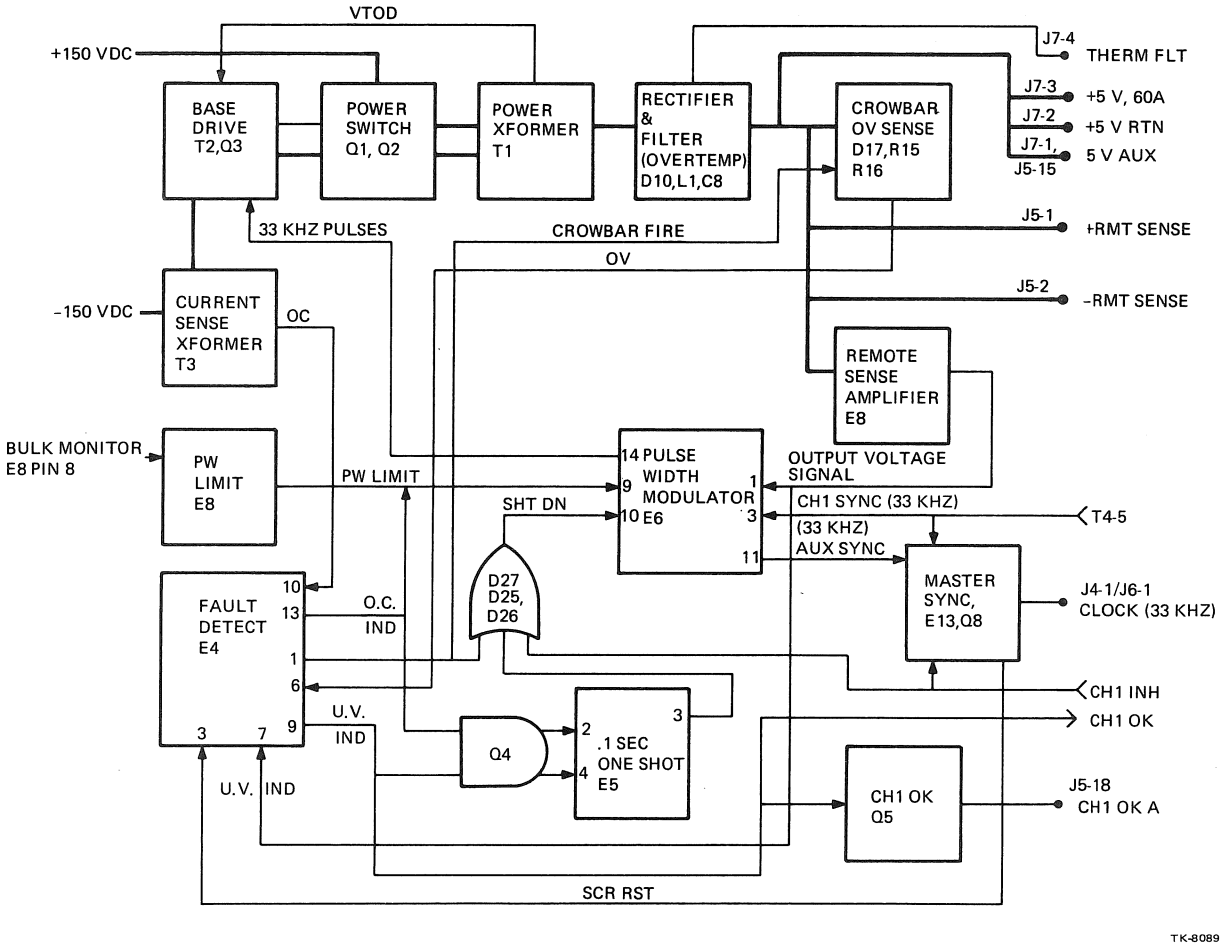


Figure 4-8 The +5.1 V Power Supply Block Diagram

When CH1 INH is deasserted, pin 10 of the pulse width modulator (E6) goes low, allowing the soft start capacitor (C22) to charge through pin 8. This permits the oscillator section of E6, operating at 66 KHz (as determined by C23 and R45) and synchronized on every other cycle by the 33 KHz CH1 SYNC pulses, to produce two 33 KHz pulses out of E6 (pin 14 and 11). These two outputs are 180° out of phase and increase in pulse width as C22 charges. E6-14 drives Q3, which drives the power switch (Q1 and Q2) through the basedrive transformer (T2). Phasing is such that when Q3 is on, Q1 and Q2 are off. When E3-14 goes high, Q3 is turned on and T2 is driven to saturation. E3-14 goes low and Q3 is turned off causing the flyback voltage produced by T2 to turn on Q1 and Q2.

Their on state is sustained at a forced Beta of 6 with T2 in a current transformer mode driven by the power switch current through windings 1-2. During their on period, Q1 and Q2 connect the BULK DC across the primary of the power transformer (T1-1,2). Voltage induced on the secondary of T1 (pins 3 and 4) is rectified by D10 and filtered by L1 and C8 becoming the +5.1 V, 60 A, output (J7-3 and J7-2). Voltage induced in the secondary of T1 at pins 6 and 7 (VTOD) charges C11 to about 60 volts.

At the end of the power switch on period, Q3 is driven on, connecting T2-7 to common. Voltage is supplied to T2-8 by C11 through R12 and D14. The energy stored in C11 ensures rapid turn off of Q1 and Q2 (< 1 μ storage time). When C11 is depleted, the +14 V through R13 and D16 ensures that T2 is driven to saturation again prior to the start of another power switch on period.

4.2.3.2 +5.1 V, 60 A Regulation – Regulation of the +5.1 V output is effected by monitoring the voltage level of the output, then varing the duty cycle of the power switch (Q1 and Q2) through the pulse width modulator (E6).

Remote sense amplifier (E8 which is a differential amplifier with a gain of 1,) monitors the output voltage at either the output of the power supply (through J7-6 and J7-7 if the remote sense is not connected) or at the point which remote sense lines (J5-1, +SENSE and J5-2, –SENSE) are connected to the load. It produces a voltage (E8-1) which represents the output voltage level referenced to common. The PWM (E6-1) accepts this voltage and varies the duty cycle of the 33 KHz pulses (pins 11 and 14) according to the voltage level.

If the output voltage increases, E8-1 increases causing E6 to decrease the duty cycle of the 33 KHz pulses. Conversely, if the output voltage decreases, E8-1 decreases causing E6 to increase the duty cycle of the 33 KHz pulses (see Appendix A). The maximum duty cycle of the 33 KHz pulse is limited between 30 and 40 percent, depending on the line voltage, by the pulse width limit circuit (E8). During low line voltage, E8-7 limits the duty cycle to a maximum of 40 percent; during high line voltage conditions, E8-14 limits the duty cycle to a maximum of 30 percent.

The varied duty cycle of the E6's 33 KHz pulses varies the duty cycle of the power switch to regulate the output.

4.2.3.3 +5.1 V Overvoltage Protection – Overvoltage protection in the +5.1 V power supply is provided by the fault detect circuit, overvoltage sense resistors, and silicon controlled rectifier (SCR).

If the power supply output reaches the overvoltage trip point of 6.5 V (overvoltage condition), the fault detect circuit (E4, see Appendix B) monitoring the supply output (pin 6) at the overvoltage sense resistors (R15 and R16) produces a high (pin 1), which shuts down the pulse width modulator E6-10 and turns the SCR (D17) on. The high on pin 1 remains present until E4-3 is pulled low. Shutdown of E6 inhibits production of the 33 KHz pulses (pin 14 stays high) and the output voltage. The SCR when biased on pulls the power supply output down to 0.7 V.

As the output voltage drops below 4.8 V, the fault detect circuit (E4) interprets an undervoltage (pin 7) from the remote sense amplifier (E8) through R33 and R34. E4-9 goes low, deasserting CH1 OK and biasing Q5 off, which deasserts CH1 OK A turning off the CH1 OK indicator (LED) on the distribution board.

The power supply stays in this condition until it is reenabled. The power supply is reenabled when the KEYSWITCH is set to OFF, then ON again. When the KEYSWITCH is set to OFF, CH1 INH is asserted, biasing Q8 on, which produces a low (SCR RST) at E4-3 resetting E4, causing pin 1 to go low. Setting the KEYSWITCH to ON enables the power supply, allowing it to produce the +5.1 V output. However, if an overvoltage condition reoccurs, this operation repeats.

4.2.3.4 +5.1 V Overcurrent Protection – Overcurrent protection in the +5.1 V power supply is provided by the fault detect and overcurrent shutdown circuits at approximately 70 amps load current.

As the load current increases, the current through the primary of the power transformer (T1-1 and 2) increases proportionally. This increase also occurs in the current sense transformer (T3). Current induced to the secondary of T3 (3-4) flows through R28 producing a voltage proportional to the load current. The fault detect circuit (E4, see Appendix B) monitoring (pin 10) the voltage across R28 produces a low at pin 13, when this voltage exceeds 2.5 volts.

This low terminates the pulse output from E6 (via D23 into E6-9). The terminated pulse output shuts off Q1 and Q2, which decreases the current through T3, causing E4-13 to go high. This allows E6 to resume producing the pulse output. However, if the overload is sufficient to cause the output to drop below 4.8 V, the low from the undervoltage section of E4 (E4-9) enables E5 through Q4.

The next overcurrent pulse from E4-13 (low) triggers E5 through pin 2. E5 is a 100 ms one shot which inhibits E6 for this period of time. After 100 ms, E6 restarts, producing gradually widening pulses on pins 14 and 11. If the overcurrent point is reached again (overload or short still present), E5 is triggered again. This continues to repeat until the overload is removed.

4.2.3.5 CLOCK Output Generation – The H7200 synchronizes all power switching circuits in the power supply configured around it, preventing interference from random frequencies. In addition, when the 5 V output is running, the CH2 (H7213) and CH3 (H7211) synchronization signals (CLOCK) occur during the off time of power switches Q1 and Q2. This allows the power switches of these modules to run out of phase with Q1 and Q2, causing a smoother flow of current from the BULK DC.

By deriving the master clock signal (CLOCK) from the positive edge of the voltage at T4-5, the pulse width modulator for the ILV power supply (E3) is the master clock.

D40, C37, R87, and R88 change the positive edge of the pulse from T4-5 to a pulse (at 33 KHz) used to synchronize E6. If E6 is inhibited (CH1 INH asserted), Q8 is turned on and pin 4 of E13 is pulled down to 2 V. This enables E13 to pass the pulses from T4-5 to pin 2 where they appear on the CLOCK pins (J4-1 and J6-1). If E6 is enabled, Q8 is off, and E13-4 is high, blocking the pulses from T4-5. Coincidently, E6-14 produces pulses which are out of phase with pin 11. The negative transistion of E6-11 is applied, through C39, to E13-6 which inverts it and sends it to the CLOCK outputs (J4-1 and J6-1) via E13-1.

4.2.4 Power Supply Control and Status Reporting

The power supply control and status reporting circuit controls the three states of the H7202B power supply: ON, OFF, and STANDBY. It indicates to the CPU which state it is in with the status signals AC LOW, DC LOW and BOOT EN. The state of the power supply indicates the output voltages available. Table 4-1 shows the states of the power supply, the output voltage available and the level of the CPU status signals in each state.

The following description is keyed to Figure 4-9 and engineering drawing CS-5413857-0-0.

4.2.4.1 OFF – The power supply goes into the OFF state when:

- Ac line voltage is lost in the ON or STANDBY state (with the optional BBU not connected).
- The VAX-11/730 front panel KEYSWITCH is set to OFF. (This removes the low on PWR REQ.)
- SHTDN at pin 1 of the DEC POWER CONTROL BUS is pulled low.
- An overtemperature switch closes in the power supply or there is no air flow in the CPU fan assembly.

Table 4-1 Power Supply States

State	Voltages Available					Status Signal Level		
	+5.1 V	+15 V	−15 V	+5.1 VB	+12.3 V	AC LOW	DC LOW	BOOT EN
OFF	NO	NO	NO	NO	NO	L	L	L
STANDBY	NO	NO	NO	YES	YES	L	L	*
ON	YES	YES	YES	YES	YES	H	H	H

* H if previous state was ON; L if previous state was OFF.

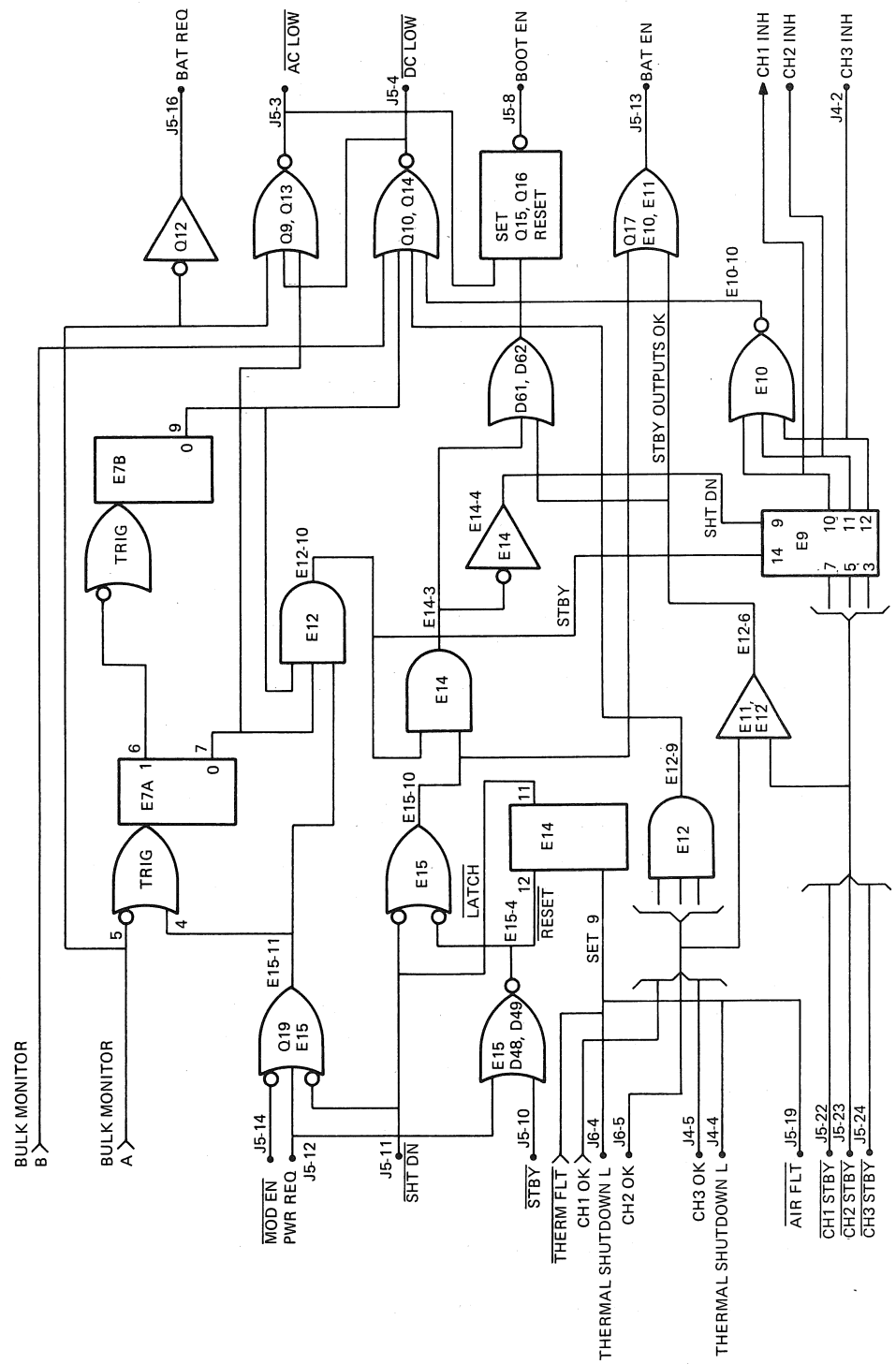


Figure 4-9 The Power Supply Control and Status Reporting Circuit Equivalence Diagram

When the ac line voltage is lost, the BULK DC is lost also. This is sensed by the BULK MONITOR circuit (Paragraph 4.2.2.3), which causes the BULK MONITOR A and B signals to go low. BULK MONITOR A goes low as the BULK DC drops below 200 volts indicating the power supply voltage outputs will remain in regulation for 6 ms. BULK MONITOR A low turns on Q12 forcing BAT EN (J5-16) high. (If the optioned BBU is connected, this signal going high would enable it to produce the battery backup power.) BULK MONITOR A also turns on Q9 (through D51), causing the cathode of D57 to go from −12.6 V to +14 V and the anode to go from −12 V to 0 V. This turns on Q13, which pulls AC LOW (J5-3) down to SIG RTN (J5-7).

NOTE

SIG RTN is connected external to the power supply to +5.1 V RTN. SIG RTN should be within .25 V of power supply circuit common.

The low transistion of BULK MONITOR A also triggers one-shot E7. E7-7 goes low and E7-6 goes high for approximately 7 ms. After 7 ms E7-7 goes high and E7-6 goes low, causing E7-9 to go low for 2 ms. This causes DC LOW to go low (thru D53 and Q10). Q10 maintains AC LOW through D58. After 2 ms E7-9 goes high. When the BULK DC drops below 175, BULK MONITOR B goes low indicating the power supply output remains in regulation for 1 ms. This causes E15-11,10 to go high (unless the power supply is in the STANDBY state, which already has E15-11 high).

Setting the KEYSWITCH to OFF or pulling SHTDN (J5-11) low causes E15-10,11 to go high (unless the power supply is in the STANDBY state, which already has E15-11 high).

When the power supply is in either the ON or STANDBY state, and either THERMAL SHUTDOWN L (thermal switch on D11 of the H7213), THERM FLT (thermal switch on the output assembly heat sink of the H7200), or AIR FLT (air flow sensor signal in the CPU fan assembly indicator) go low, E14-11 goes low. This causes E15-11,10 to go high (unless the power supply is in the STANDBY state, which already has E15-11 high).

E15-11,10 going high results in the logic levels for the following path: E12-10 H (after E7A and E7B have timed out), E14-4 H and E9-14,9 H. When E14-3 goes low, Q15 and Q16 are turned on, pulling BOOT EN (J5-8) down to SIG RTN (J5-7). E9 is a selectable gate whose output levels depend upon which inputs are selected by the select signal. If E9-9 (KA) is high, the levels at pins 2, 4, and 6 (A inputs) are transmitted to pins 10-12 (D outputs), respectively.

If E9-14 (KB) is high, the levels at pins 7, 5, and 3 (B inputs) are transmitted to pins 10-12 (D outputs), respectively. The levels of the A inputs are fixed at +14 V, but the levels of the B inputs are determined by a jumper built into P3 of the flexprint that connects J5-21, 22, and 24. This jumper connects CH1 STBY (J5-22) and CH3 STBY (J5-24) to +14 V. If both E9-9 and E9-14 are high, any high input (A or B) gives a respective high output. If both E9-9 and E9-14 are low, the outputs are low. Since both E9-14 and E9-9 are high in the preceding case, the E9-10,11,12 are high (CH1 INH , CH2 INH and CH3 INH are all high). This disables all power modules from producing output voltages and causes E10-10 to go low keeping AC LOW and DC LOW low.

4.2.4.2 STANDBY – The power supply goes into the STANDBY state when:

- The VAX-11/730 front panel KEYSWITCH is set to STD BY.
- The AC line voltage is lost in the STD BY or ON state with the optional BBU connected.

Setting the KEYSWITCH to STD BY connects STBY (J5-10) to BUS RTN (J5-9) and results in the following signal path and logic levels: E15-5,6 L, E15-1,2 H, E15-3,12 L, E15-11 H, E15-4 H, and E15-10 L. If the KEYSWITCH was in any position except OFF before STAND BY, a high at E15-11 obtains the same results as BULK MONITOR A going low (Paragraph 4.2.4.1): E7-7,9 goes from high to low then back to high in sequence, which causes E12-10 and E9-14 to go high. E7-7,9 going low causes AC LOW and DC LOW to go low (Paragraph 4.2.4.1).

If the KEYSWITCH was in the OFF position before STANDBY, a high at E15-11 has no effect on E7, since E15-11 is already high and AC LOW and DC LOW are already low. Also, E12-10 and E9-14 are already high. E12-10 high and E15-10 low causes E14-4 and E9-9 to go low. When E9-9 is low and E9-14 is high, E9-10,12 are high (CH1 INH and CH3 INH high) and E9-11 is low (CH2 INH low), which enables the memory power module to produce the output voltages. If the KEYSWITCH was in any position except OFF before STAND BY, BOOT EN remains high. However, if the KEYSWITCH was in the OFF state, BOOT EN would stay low.

When the ac line voltage is lost, the BULK DC decreases as C1 and C2 discharges. As it goes below 200 V, the circuit (Paragraph 4.2.2.3) causes the BULK MONITOR A signal to go low. If the power supply is in the ON state, AC LOW and DC LOW go low. However, if the power supply was in STANDBY, AC LOW and DC LOW are already low. BULK MONITOR A going low turns on Q12, forcing BAT REQ high (J5-16) which enables the connected BBU to supply the battery backup power (BULK DC).

The BBU forces MOD EN (J5-14) low, which turns on Q19. Q19 on causes E15-11 to go high (unless the power supply is already in the STANDBY state, in which case E15-11 would already be high). If the BBU is not connected, C1 and C2 continue to discharge. At 175 V, BULK MONITOR B goes low which maintains or reasserts DC LOW through D54 and pulls E15-9,13 L through D24. This causes the logic levels for the following signal path: E15-11 H, E12-10 H, E14-4 H, and E9-14,10,11,12 H, shutting off all outputs.

4.2.4.3 ON – The power supply goes into the ON state when:

- The VAX-11/730 front panel KEYSWITCH is set to any position except OFF or STANDBY.
- PWR REQ is pulled low at pin 2 of the DEC POWER CONTROL BUS.

Either condition connects PWR REQ (J5-12) to BUS RTN (J5-9). A low on PWR REQ places a low on STBY (thru D48). This results in the following signal path and logic levels: E15-3 H, E15-11 L, E12-10 L, E9-14 L, and E9-10,11,12 L. Pins 10, 11, and 12 going low enables all three power modules to produce the output voltages.

CH1 OK, CH2 OK, and CH3 OK go high (power module output voltages with in regulation) causing E12-9 to go high, turning off Q10. Q10 off allows DC LOW to go high (after a small delay provided by C49) and AC LOW to go high (after a longer delay provided by C48). The CH OK signals going high also produce E12-6 H which drives BAT EN high through E10B, E11D, and Q7. E12-6 causes the gate of Q15 to be pulled high by AC LOW (through D60) by remaining low on the cathode of D61. This causes BOOT EN to go high.

4.3 MEMORY POWER MODULE (H7213)

The memory power module contains the memory power supply which accepts the BULK DC to generate and regulate the +5 VB, 15 A, and +12.3 V, 3 A, outputs. The following description is keyed to Figure 4-10 and engineering drawing 5413869.

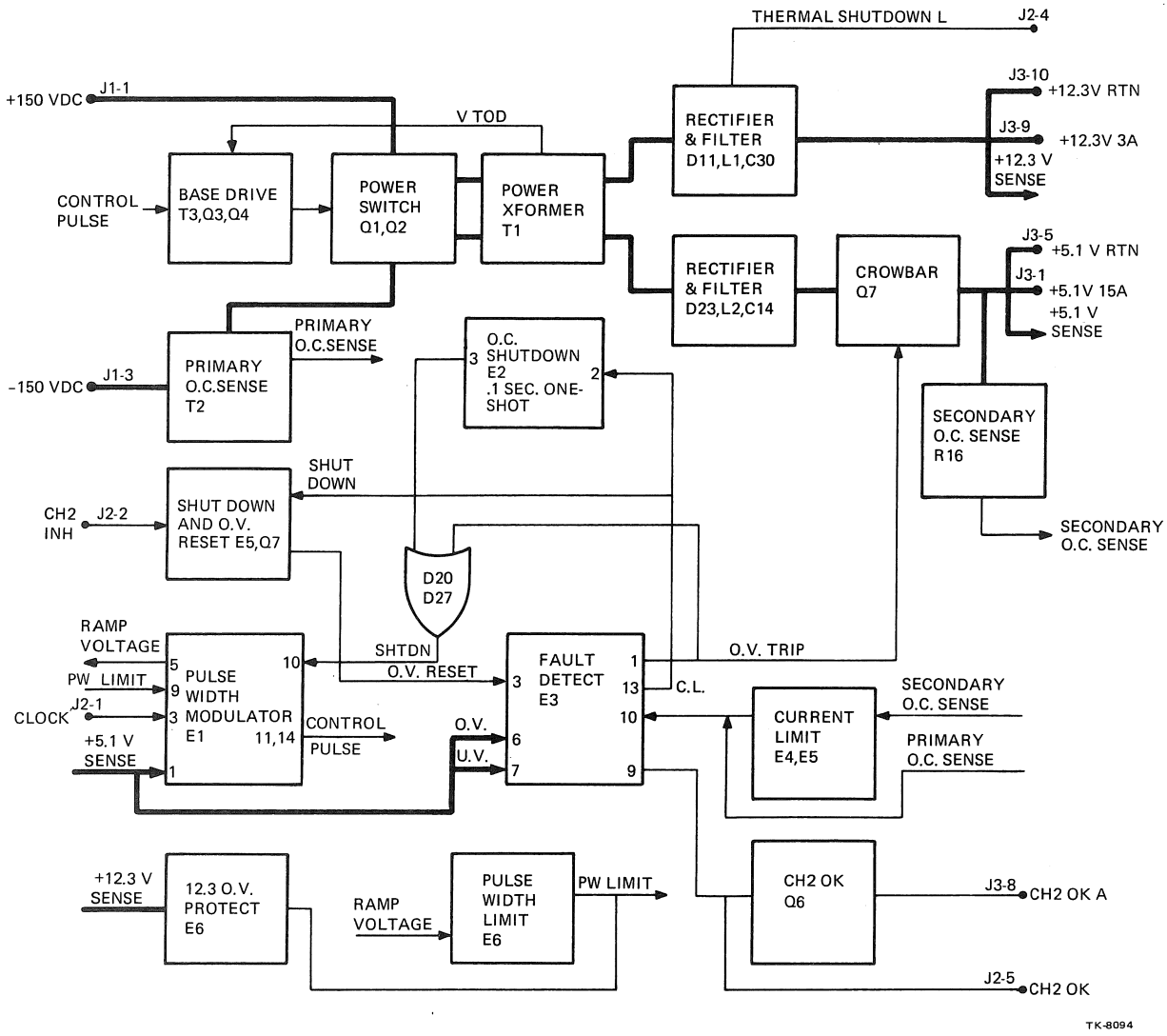


Figure 4-10 The H7213 Memory Power Module Block Diagram

4.3.1 +5 VB, 15 A, and +12.3 V, 3 A, Generation

The +5 VB, 15 A, and +12.3 V, 3 A are derived from the BULK DC by a pulse width modulated forward converter operating at 33 KHz.

The memory power supply generates the +5.1 VB and +12.3 V outputs when the CH2 INH signal (from the power supply control and status reporting circuit) is deasserted.

When CH2 INH (J2-2) is deasserted, Q7 is biased off, causing E2-2 to go low. This low causes E2-3 to go low causing the pulse width modulator (E1, see Appendix A) pin 10 to go low and the soft start capacitor (C22) to charge through pin 8. This allows the ramp generator (C27, C23 and R36) at pin 5 and 33 KHz CLOCK signal at pin 3 to produce the 33 KHz pulses (CONTROL PULSE) out of E1 at pins 11 and 14, which increases in pulse width as C22 charges. This CONTROL PULSE is synchronized to the ILV pulse width modulator by the 33 KHz CLOCK signal. When the CONTROL PULSE goes high, Q4 is biased on, which biases Q3 on, driving the primary (pin 7 and 8) of the base drive transformer (T3) from the energy stored in C3.

Voltage induced to the secondary (pins 5 and 3) of T3 drives Q1 and Q2 off. When the CONTROL PULSE goes low, Q4 and Q3 are biased off. Energy stored in T3 changes polarity and the voltage induced on the secondary (pins 5 and 3) of T3 biases Q1 and Q2 on. Q1 and Q2 biased on, drops the BULK DC across the primary of T1. Voltage induced to the secondary of T1 at pin 4 is rectified by D23 and filtered by L2 and C14 to become the +5.1 VB output (J3-1 and J3-5). Voltage induced to the secondary of T1 at pin 6 is rectified by D11 and filtered by L1 and C30 to become the +12.3 V output (J3-9 and J3-10). Voltage induced to the secondary of T1 at pin 8 charges C3 which supplies the turn-off drive.

4.3.2 +5.1 VB, 15 A, and +12.3 V, 3 A Regulation

Regulation of the +5.1 VB and +12.3 V outputs is effected by monitoring the voltage level of the +5.1 VB output, then varying the duty cycle of the power switch through the pulse width modulator (E1).

The pulse width modulator (E1) monitors (pin 1) the +5.1 V SENSE line and varies the duty cycle of the power switch by increasing or decreasing the duty cycle of its 33 KHz pulses, as the SENSE line voltage decreases or increases. If the +5.1 V SENSE line voltage increases, E1 deceases the duty cycle of the 33 KHz pulses, which decreases the duty cycle of the power switch and lowers the energy delivered to the output.

Conversely, if the +5.1 V SENSE line voltage decreases, E1 increases the duty cycle of the 33 KHz pulses, which increases the duty cycle of the power switch and increases the the energy delivered to the output. However, the duty cycle of the 33 KHz pulses is limited by the pulse width limit circuit (E6). E6 intergrates E1's ramp voltage to produce clamp voltage at E6-1. This limits the output of E1's error amplifier (E1-9), limiting the 33 KHz pulses duty cycle to 45 percent.

4.3.3 Overvoltage Protection

Overvoltage protection in the memory power supply is provided separately for the +5.1 VB and +12.3 V outputs.

4.3.3.1 +5.1 VB Overvoltage Protection – Protection against +5.1 VB output overvoltage is provided by the fault detect and crowbar circuits.

If overvoltage condition occurs in the +5.1 VB output, the pulse width modulator is inhibited and the output voltage level is decreased. If the +5.1 VB output voltage level rises to the 5.7 V overvoltage trip point (overvoltage condition), the fault detect circuit (E3, see Appendix B), monitoring (pin 6) the +5.1 V SENSE line through R41 and R42, goes high. This high (OV TRIP) inhibits the pulse width modulator (E1) and biases the crowbar D19 on. D19 biased on pulls the +5.1 VB output down to 0.7 V.

When the +5.1 VB output drops below 4.5 V, the fault detect circuit deasserts the CH2 OK and CH2 OK A signals. The fault detect circuit (E3) monitoring (pin 7) the +5.1 V SENSE line, through R41, interprets drop in output voltage as an undervoltage and produces a low at pin 9. This low is the deasserted CH2 OK signal (at J2,-5) which biases Q6 off, deasserting the CH2 OK A signal (at J3,-8). CH2 OK A deasserted turns off the CH2 OK indicator (LED) on the distribution board.

The power supply remains in this condition until it is reenabled. The power supply is reenabled when the KEYSWITCH is set to OFF, then set to ON (or STANDBY). When the KEYSWITCH is set to OFF, CH2 INH is asserted, biasing Q7 on, which causes E5-7 to go low. This low is applied to E5-3, resetting it. Resetting E4 causes pin 1 to go low, which biases D19 off and enables E1 to produce the CONTROL PULSE when the KEYSWITCH is set to ON (or STANDBY). Setting the KEYSWITCH to ON (or STANDBY) enables the power supply to produce the +5.1 VB and +12.3 V outputs.

4.3.3.2 +12.3 V Overvoltage Protection – Under normal load conditions (normal load on the +12.3 V output is above 0.75 amps), overvoltage in the +12.3 V output is interpreted as overvoltage in the +5.1 VB output, and is managed as described in Paragraph 4.3.3.1. If the +12.3 V output load drops below 0.75 amps, output overvoltage occurs and overvoltage protection is provided by the +12.3 V overvoltage protection circuit.

If the +12.3 V output load drops below 0.75 amps, the output voltage level rises to the overvoltage trip point of 15 V. The +12.3 V overvoltage protection circuit (E6) decreases the output voltage level below 15 V by decreasing the duty cycle of the power switch. When the output voltage level reaches 15 V, E6-7 goes low. This low is applied to E1-9, decreasing the duty cycle of the CONTROL PULSE, which decreases the duty cycle of Q1 and Q2, which in turn decreases the output voltage to less than 15 V.

This operation results in a depressed 5.1 VB output and continues until the output load rises above 0.75 amps.

4.3.4 Overcurrent Protection

Overcurrent protection in the memory power module is provided by the primary overcurrent sense, secondary overcurrent sense, current limit, fault detect, and overcurrent shutdown circuits.

Overcurrents in the memory power supply are either determined at the primary of the power transformer or at the +12.3 V output. Overcurrent is determined at the primary of the power transformer when the +12.3 V output load does not exceed 7 amps. Conversely, overcurrent is determined at the +12.3 V output if that output load exceeds 7 amps.

If the +5.1 VB output exceeds the overcurrent starting point, the primary overcurrent sense, fault detect, and overcurrent shutdown circuits inhibit the operation of the pulse width modulator. When the +5.1 V output load exceeds 19 amps (the overcurrent starting point), the current through the primary of the power transformer (T1) increases.

This current increase is out of the current sense transformer (T2) which is seen as an increasing voltage across R9. This increased voltage, through the fault detect circuit (E3, see Appendix B), causes pin 3 of the overcurrent shutdown circuit (E2), to go high for .1 second, disabling the operation of pulse width modulator (E1) which internally discharges the soft start capacitor (C22).

When E1 is disabled, the output voltage drops. These drops are interpreted as undervoltage conditions the CH2 OK and CH2 OK A signals then deasserted as described in Paragraph 4.3.3.1.

If the +12.3 V output exceeds the overcurrent starting point, the secondary overcurrent sense, current limit, fault detect, and overcurrent shutdown circuits, inhibit the operation of the pulse width modulator. The +12.3 V output load is monitored by the voltage across the secondary overcurrent sense resistor (R16), SEC OC SENSE A is tied to the +5.1 VB output, SEC OC SENSE B becomes more negative with respect to this as the load current increases.

These signals are applied to E4-2,4 which is set for a gain of −30.1. E4-1 increases 1.2 V for every ampere of the +12.3 V output load current. This voltage increases the primary overcurrent threshold through R25 and is supplied to comparator E5-3. At a load of approximately 7 A, E5-1 goes high. This is supplied to E3-10, which causes E3-13 to go low, triggering .1 second one-shot E2. E2 then shuts down E1. After .1 second, this circuit restarts. If the output reaches overcurrent again, it shuts down again.

4.4 H7211 COMMUNICATIONS POWER MODULE

The communications power module contains the communications power supply which accepts the BULK DC to generate and regulate the +15 V, 2 A and the −15 V, 3 A outputs. The following description is keyed to Figure 4-11 and engineering drawing 5413867.

4.4.1 +15 V, 2 A and −15 V, 3 A Generation

The +15 V, 2 A and −15 V, 3 A outputs are derived from the BULK DC by a pulse width modulated flyback converter operating at 33 KHz, switching the BULK DC across the primary of the power transformer then, rectifying and filtering the voltage induced on the secondary. This switching is performed by the power switch, which is controlled through the base drive by the pulse width modulator's 33 KHz pulses (TN OFF DR).

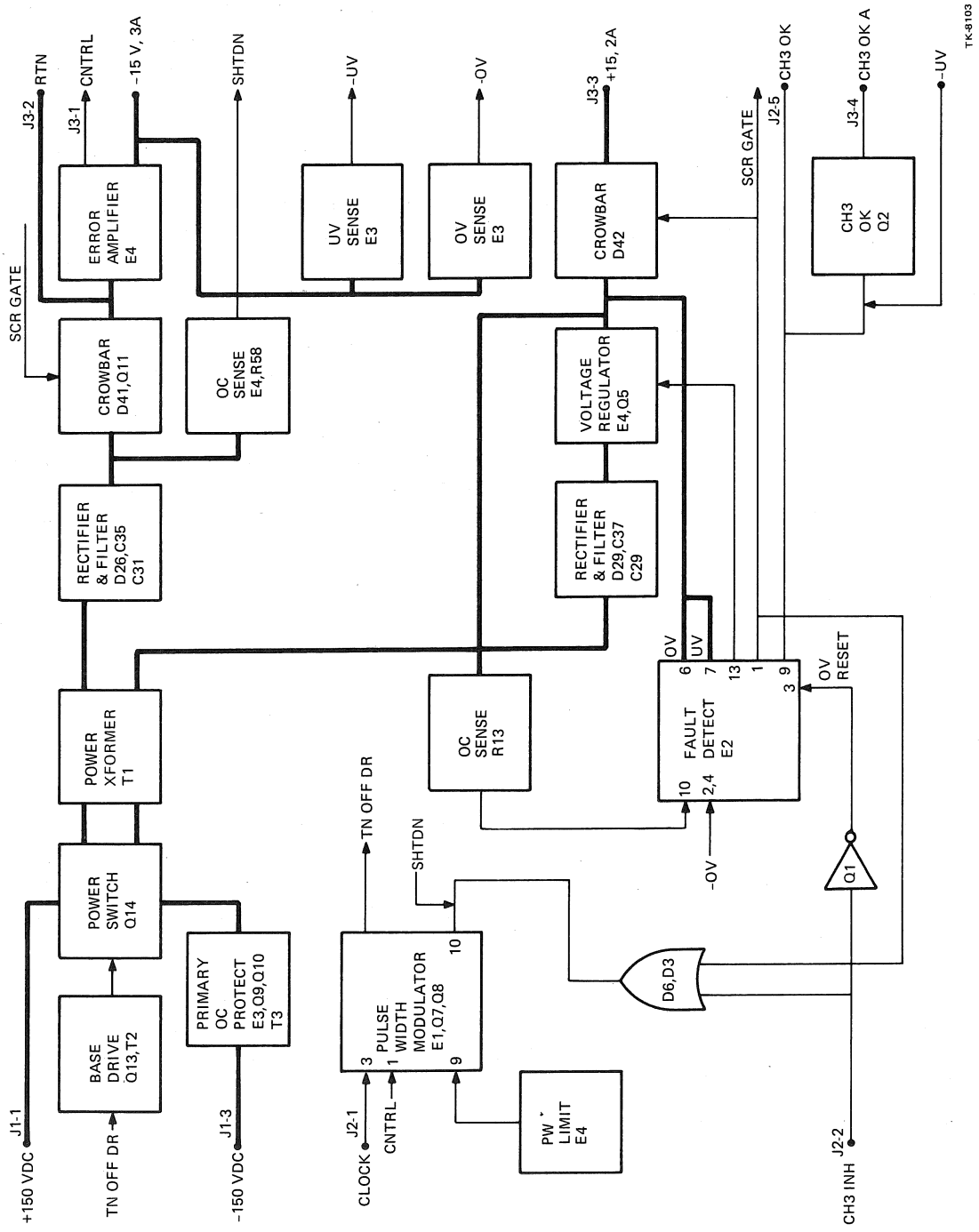


Figure 4-11 The H7211 Communication Power Module Block Diagram

The pulse width modulator (E1, Q7, and Q8) generates the 33 KHz pulses when the CH3 INH signal (from the power supply control and status reporting circuit) is deasserted.

When CH3 INH (J2-2) is deasserted by the power supply control circuit on the H7200, pin 10 of the pulse width modulator (E1, see Appendix A) goes low, allowing the soft start capacitor (C12) to charge through pin 8. This allows the ramp generator (C13 and C14 at pin 5) and the 33 KHz CLOCK (pin 3) signal to produce the 33 KHz pulses (TN OFF DR) out of E1, at the junction of pins 11 and 14. This TN OFF DR, which is in phase with the ILV voltage, increases in pulse width as C12 charges.

The TN OFF DN signal biases the power switch (Q14) on and off, to switch the BULK DC through the power transformer (T1), generating the +15 V, 2 A and −15 V, 2A and −15 V, 3 A outputs. When the TN OFF DR signal goes high (Q7 biased on), Q13 is biased on, driving the primary of T2 (pins 6 and 5) from C36 or +14 V through R72. Voltage induced on the secondary of T2 causes pin 3 to go low, biasing Q14 off. When the TN OFF DR signal goes low (Q8 biased on), Q13 is biased off and the energy stored in T2 changes polarity.

Voltage induced on the secondary of T2 causes pin 3 to go high, biasing Q14 on. Q14 biased on drops the BULK DC across the primary of T1. Voltage induced to the secondary of T1-3,5 biases D26 and D29 off. Voltage induced to the secondary of T1-10 charges C36. When the TN OFF DR signal again goes high, Q13 is biased on, which discharges C36 through the primary of T2. These two voltages are induced to the secondary of T2 biasing Q14 off. This causes the energy stored in T1 to change polarity. Voltage induced to the secondary of T1 at pin 3 is rectified by D26 and filtered by C35 to become the −15 V, 3 A output. Voltage induced to the secondary of T1 at pin 5 is rectified by D29 and filtered by C37 to become the +15 V, 2 A output.

4.4.2 −15 V, 3 A, and +15 V ,2 A Regulation

Output regulation in the communications power supply is provided separately for the −15 V, 3 A and +15 V, 2 A outputs.

4.4.2.1 −15 V, 3 A Regulation – The −15 V, 3 A output is regulated by monitoring the voltage level of that output, then varying the duty cycle of the power switch through the pulse width modulator (E1).

The error amplifier (E4) monitors the −15 V output and produces an error voltage which varies the duty cycle of the 33 KHz pulses (TN OFF DR) from the pulse width modulator (E1, see Appendix A). If the −15 V output voltage increases (becomes more negative) the error voltage (CNTRL) from E4-7 increases (positive). This increased voltage, which is applied to E1-1, decreases the duty cycle of the 33 KHz pulses. Conversely, if the output voltage decreases (becomes less negative) the error voltage from E4-7 decreases. This decreased voltage increases the duty cycle of the 33 KHz pulses.

The varied duty cycle of the 33 KHz pulses from E4, varies the duty cycle of the power switch (Q14), to increase or decrease the −15 V output. If the duty cycle of the 33 KHz pulses decreases, the duty cycle of Q14 increases, which decreases the −15 V output. If the duty cycle of the 33 KHz pulses increases, the duty cycle of Q14 decreases, which increases the −15 V output.

4.4.3 +15 V, 2 A Regulation

The +15 V output is regulated by monitoring the the voltage level of that output, then increasing or decreasing the conduction of Q5 to keep that output within its voltage levels.

The voltage regulator (E4 and Q5) monitors the +15 V output at the junction of R27 and R26 and varies the conduction of Q5 which varies the output voltage. If the +15 V output increases, E4-14 goes lower, decreasing the biasing of Q5 and increasing the resistance of the return path. This decreases the output voltage. If the +15 V output increases, E4-14 goes higher, increasing the biasing of Q5 and decreasing the resistance of the return path. This increases the output voltage.

4.4.4 –15 V and +15 V Overvoltage Protection

Overvoltage protection in the communications power supply is provided separately for the –15 V and +15 V outputs.

4.4.4.1 –15 V Overvoltage Protection – Protection against –15 V output overvoltage is provided by the overvoltage sense, fault detect, and crowbar circuits.

If overvoltage occurs in the –15 V output, the pulse width modulator is inhibited and the output voltage is decreased. If the –15 V output voltage level rises above the overvoltage trip point of 18 V, the overvoltage sense circuit (E3 and Q12) produces a low. The fault detect circuit (E2, see Appendix B) accepts this low (pin 4 and 2) and produces a high at pin 1. This high (SCR GATE) inhibits the pulse width modulator (E1) and biases the crowbar diodes D41 and D42 on. D41 and D42 biased on, pulls both output voltage levels down to 0.7 volts.

When the –15 V output drops below –13.3 V, undervoltage sense circuit deasserts the CH3 OK and CH3 OK A siganls. The undervoltage sense (E3) interprets the drop in output voltage as an undervoltage condition and produces a low at pin 14. This low biases Q2 off, deasserting the CH 3 OK (J2-5) and CH3 OK A (J3-4) signals. CH3 OK A deasserted turns off the CH3 OK indicator (distribution board LED).

The power supply remains in this condition until it is reenabled. The power supply is reenabled when the KEYSWITCH is set to OFF, then set to ON. When the KEYSWITCH is set to OFF, CH3 INH is asserted, biasing Q1 on. Q1 biased on applies a low to pin 3 of the fault detect circuit (E2), causing pin 1 to produce a low. This low biases D29 and D26 off. When the KEYSWITCH is set to ON, CH3 INH is deasserted, allowing the pulse width modulator (E1) to produce the 33 KHz pulses and E2 to bias Q2 on, asserting the CH3 OK and CH3 OK A signals if the outputs remain in their regulation band.

4.4.4.2 +15 V Overvoltage Protection – Protection against +15 V output overvoltage is provided by the fault detect and crowbar circuits.

If overvoltage occurs in the +15 V output, the pulse width modulator is inhibited and the output voltage is decreased. If the +15 V output voltage rises above the overvoltage trip point of 18 V, the fault detect circuit (E2, see Appendix B) produces a high at pin 1. This high (SCR GATE) disables the pulse width modulator (E1) and biases the crowbar diodes (D42 and D41) on. D42 and D41 biased on, pull both output voltage levels down to 0.7 V.

When the +15 V output drops below +13.5 V, E2 interprets this as undervoltage and produces a low at pin 9. This low is the deasserted CH3 OK signal and biases Q2 off, deasserting the CH3 OK A signal.

The power module remains in this condition until it is reenabled. The power supply is reenabled when the KEYSWITCH is set to OFF, then set to ON. When the KEYSWITCH is set to OFF, CH3 INH is asserted, biasing Q1 on. Q1 biased on applies a low to pin 3 of the fault detect circuit (E2) causing pin 1 to produce a low. This low biases D29 and D26 off. When the KEYSWITCH is set to ON, CH3 INH is deasserted, allowing the pulse width modulator (E1) to produce the 33 KHz pulses and E2 to bias Q2 on, asserting the CH3 OK and CH3 OK A signals if the outputs remain in their regulation band.

4.4.5 –15 V and +15 V Overcurrent Protection

Overcurrent protection in the communications power supply is provided in the primary of the power transformer and separately for the –15 V and +15 V outputs.

4.4.5.1 Primary Overcurrent Protection – Overcurrent protection in the primary of the power transformer is provided by the primary overcurrent protection circuit.

When current in the primary of the power transformer becomes excessive, the primary overcurrent protection circuit terminates the on pulse of the power switch. As the current through the primary of the power transformer (T1) increases, current through the primary of the current sense transformer (T3) increases. This increase is translated by D18 as an increase in voltage across the secondary of T3. E3-7 monitoring the voltage across the secondary of T3 produces a high at pin 1.

This high biases Q9 off, allowing C33 to charge to 5.1 V. As C33 charges, E3-13 goes high. E3-13 going high holds pin 1 high. D23 is biased on, which biases Q10 on. Q10 biased on biases Q13 on, which biases Q14 off. When the charge voltage across C33 reaches 2.5 V (10 us), E3-13 goes low. This low causes E3-1 to go low, biasing Q9 on. Q9 biased on, biases D23 off, which biases Q10 off. By this time, Q13 is driven by the TN OFF DR signal, so Q14 does not turn on until the next normal cycle. This operation repeats until the excessive current no longer exists in the primary of T1.

4.4.5.2 −15 V Overcurrent Protection – Overcurrent protection in the −15 V output is provided by the −15 V overcurrent sense circuit.

If the −15 V output current exceeds the overcurrent starting point (3.3 A), or if the output current exceeds 1.5 A when the output voltage is low, E4 compares the voltage across R58 with the 5.1 V reference to produce a high out of pin 1. This high (SHTDN) disables the pulse width modulator (E1). The output current remains at 1.5 A until the output overcurrent no longer exists.

When the output voltage drops below the undervoltage trip point, the CH3 OK and CH3 OK A signals are deasserted as described in Paragraph 4.4.4.1.

4.4.5.3 +15 V, 2 A Overcurrent Protection – Overcurrent protection in the +15 V output is provided by the overcurrent sense, fault detect, and voltage regulator circuits.

If the +15 V output current exceeds the overcurrent initiation point (2.3 A), or if the output current exceeds 0.5 A (the output is shorted to ground), the fault detect circuit (E2-10) compares the negative voltage across the overcurrent sense resistor (R13) to the output voltage through R15 and D4, and produces a high at pin 13. This high causes E4-14 to go lower, which biases Q5 on less, to reduce the output current to 0.5 A (at 0 V). The output current remains at .5 A until the overcurrent no longer exists.

When the output voltage drops below the undervoltage trip point, the CH3 OK and CH3 OK A signals are deasserted as described in Paragraph 4.4.4.2.

APPENDIX A
3525A AND 3527A BLOCK DESCRIPTION

The 3525A and 3527A are complete pulse width modulators which are contained in 16 pin DIPs. The only difference between the two is that the outputs of the 3525A are low in the off state and the outputs of the 3527A are high in the off state. Refering to Figure A-1, the function of each block is listed below.

1. The REFERENCE REGULATOR provides a stable 5.1 V output to pin 16.

2. U.V. LOCKOUT holds the outputs in the off state until pin 15 (V IN) is above 8 V.

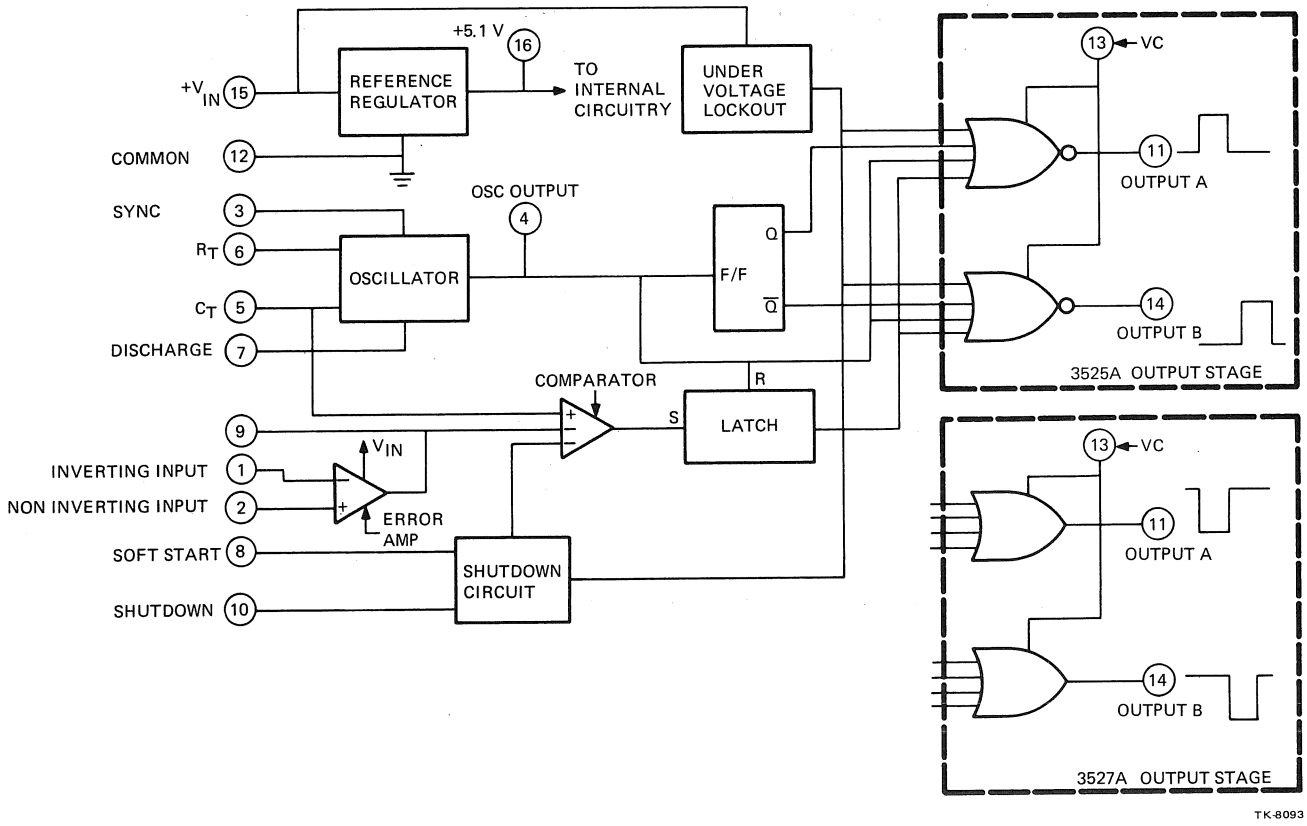


Figure A-1 Block Diagrams of the 3525A and 3527A Pulse Width Modulators

3. The OSCILLATOR is programmed by an external resistor and capacitor network connected from pins 5 (C T) and 6 (R T) to common (pin 12 COMMON). It produces a fixed frequency sawtooth waveform with (typically) .9 V at the bottom and 3.3 V at the top. This appears at pin 5 and is internally applied to the positive input of the COMPARATOR section. The OSCILLATOR may be synchronized to a higher frequency by adding synchronizing pulses to pin 3 (SYNC). It also produces pulses at pin 4 (OSC OUTPUT) which can be used to synchronize the circuit at its frequency.

4. The flip-flop (F/F) inhibits OUTPUT A (pin 11) for one oscillator period, then inhibits OUTPUT B (pin 14) for the next oscillator period. This causes each output to operate at one-half the oscillator frequency with the leading edge of the pulse of one occurring in the middle of the pulse of the other. The maximum width of each pulse is less than 50 percent of the output period. The outputs of the 3527A can be ORed together to create one output capable of nearly 100 percent duty cycle at the same frequency as the OSCILLATOR. This is done on the H7211 and H7213 power modules however, in these circuits the error amplifier output is clamped to limit the duty cycle.

5. The OUTPUT stages are capable of sourcing or sinking 100 mA. Pin 13 (V C) supplies the source (pull up) voltage which may be different than the source voltage at pin 15 (V IN).

6. The ERROR AMPLIFIER is self-explanatory and provides all the gain and bandwidth normally needed to achieve good regulation and response. In the circuit, it is connected to decrease its output as the power supply output rises. Its output feeds the COMPARATOR.

7. The COMPARATOR compares the level of the error amplifier output to the sawtooth, to decrease its pulse output as ERROR AMPLIFIER outputs decrease (refer to Figure A-2).

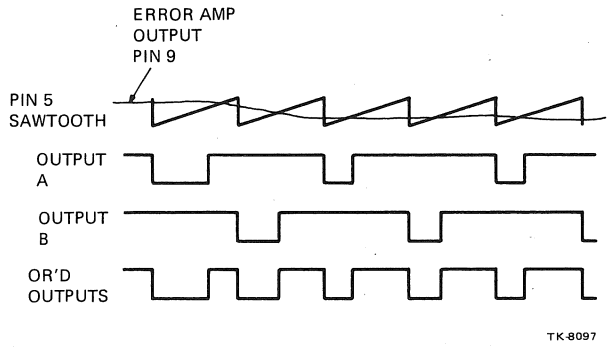


Figure A-2 Input Waveforms Compared to Output Waveforms for the 3525A and 3527A

APPENDIX B
3543 BLOCK DESCRIPTION

The 3543 is the power supply supervisory circuit used to monitor overvoltage, undervoltage and current. Refer to Figure B-1 for the functions listed below.

1. A 2.5 V reference regulator (2.5) is connected to both the overvoltage comparator (OV) and the undervoltage comparator (UV) and is also available externally at pin 15 (2.5 V REF).

2. The UV senses the voltage on pin 7 (UNDERVOLTAGE SENSE) and trips any time that voltage drops below 2.5 V. A delay (DLY) can be programmed by connecting a capacitor to pin 8 (UV DLY). This delay ignores momentary undervoltages at pin 9 (UNDERVOLTAGE INDICATION). Using an external divider, any low voltage threshold above 2.5 V can be monitored.

3. The OV operates similarly to the UV. It is activated any time pin 6 (OVERVOLTAGE SENSE) rises above 2.5 V. Its delay (DLY) is programmed by a capacitor on pin 5 (OV DLY). It contains a 200 mA SCR driver (pin 1 SCR DRIVE) for a crowbar circuit, a remote set activator (pin 2 REMOTE SET) which can latch the circuit in the fault state by connecting it to pin 4 (OVERVOLTAGE INDICATOR), and a reset pin (pin 3 RESET) to unlatch the outputs.

4. The current limit amplifier (CL) can be used either as an amplifier or in conjunction with the reference voltage as a comparator to accomplish whatever circuit function is necessary.

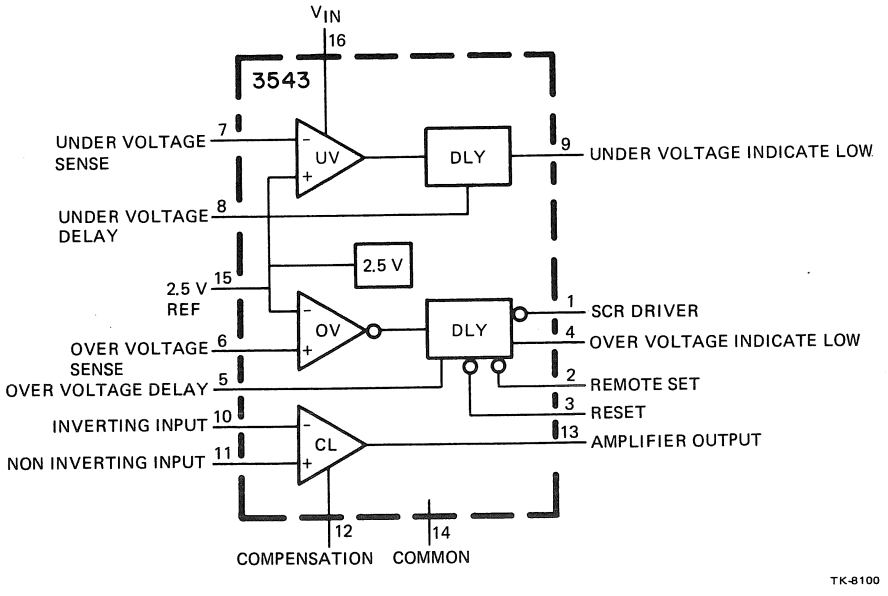


Figure B-1 Block Diagram of the 3543

H7202B Power System
Technical Description
EK-PS730-TD-001

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