Interfacing the DP8432V and the 68040

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INTRODUCTION

This application note shows how to interface the DP8432V-33 DRAM controller with Motorola's 68040 microprocessor. The reader should be familiar with the 68040 and the DP8432V modes of operation. This application note is also applicable to the DP8431V/30V. The nature of this application note is to provide an idea of a possible interface to the DP8432V. After reading this application note, the reader must analize his/her particular application and requirements.

This application note design operates at 33 MHz and supports ''Cache Line Filling'' during read cycles. It inserts 3 wait states during opening accesses, and 1 wait state during Burst Inhibit Cache Fill Accesses. The memory is interleaved every 4 double words (16 bytes) between two banks. The memory is organized in 2 Banks of 32 bits in width. Using 4M X 1 DRAMs, this arrangement gives a total memory of 32 Mb. This design uses DRAMs with output enable, thus transceivers in the data bus are not necessary. If 4 Banks were used, the total memory could be increased to 64 Mb, however, the timing calculations must then be revised due to the heavier capacitive load on the output drivers.

Four timing waveforms are presented.

1. Non Delayed Back to Back Accesses to Different Banks. It shows two opening accesses, one to each bank. (Memory Interleaving.)
2. Delayed Back to Back Access to the Same Bank. Access-Precharge-Access.
3. Burst Inhibited Cache Line Fill. Four accesses to the same bank. Fastest way of access, it transfers 16 bytes in a 5-3-3-3 fashion.
4. Refresh Cycle Arbitration.

The glue logic is implemented using a 10 ns PAL to optimize timing in a 33 MHz application. Using a PAL also reduces component count.

DESCRIPTION

Resetting and Programming. Resetting the DP8432V is accomplished by asserting $\overline{RESET}$ for at least 16 positive edges of clock. The controller is programmed during the first memory write after a system reset. During this time $\overline{RESET}$ is low the $\overline{ML}$ input is also low. During the first memory write, the 68040 puts an address to a location equal to the programming selection. $\overline{WR}$ and $\overline{AREQ}$ will assert at the beginning of the access. When $\overline{AREQ}$ goes low, the programming bits affecting the wait logic become valid, allowing $\overline{DTACK}$ to assert and the 68040 to finish the access. $\overline{WR}$ negates at the end of the access and then drives $\overline{ML}$ high. At this time the rest of the programming bits take effect and the 60 ms initialization period begins.

Non-Delayed Opening Accesses. An access begins when the 68040 places a valid address onto the address bus and asserts $\overline{TS}$. Due to the delay from BCLK high to $\overline{TS}$ asserted (19 ns max for parameter 13 in the 68040 data sheet), $\overline{TS}$ must be latch from the 68040 and asserted early enough in T2 to meet $\overline{ADS}$ asserted to CLK high (parameter 400 in the DP8432V data sheet).

The DRAM controller will assert $\overline{RAS}$ from $\overline{AREQ}$ and $\overline{ADS}$ asserted to latch the row address into the DRAM. The controller guarantees the programmed Row Address Hold Time, t_{RAH}, before switching the internal multiplexor to place the column address onto the Q outputs. The controller guarantees the programmed Column Address Set Up Time, t_{ASC}, before asserting $\overline{CAS}$ to latch the column address into the DRAM. $\overline{DTACK}$ is programmed to assert from the rising edge of T4 for normal access (1T R2=1, R3=0 plus 1T by $\overline{WAITIN}$). $\overline{TA}$ will assert from the rising edge of T5 through a registered output from the PAL. It takes 5 clock periods (~151 ns) to complete a non-delayed or opening access.

If the 68040 is to perform a single access, SIZ0 and SIZ1 will drive or keep LineTx (internal signal in the PAL16R6) low. LineTx and $\overline{TA}$ low will negate $\overline{AREQ}$ and $\overline{ADS}$ finishing the access.

Delayed Accesses. If the CPU requests an access in the middle of a refresh cycle, or if there are back to back accesses to the same bank, then the DRAM controller will delay the requested access to guarantee the required precharge time. In this application note, the DP8432V is programmed to guarantee 3 positive edges of CLK for precharge.

During most accesses, $\overline{RAS}$ negates just before the positive edge of T2 (second access). In this case, the T2 positive edge of CLK will count as the first positive clock of precharge. If worst case timing occurs (PAL delay and $\overline{AREQ}$ negated to $\overline{RAS}$ negated), $\overline{RAS}$ may negate just after the positive edge of T2 (second access). In this case precharge will take longer.

Most of the time, delayed back to back accesses take 7 clocks instead of 8 clocks (worst case time analysis). Programming 3Ts of precharge guarantees that precharge will be met in all cases. If 2Ts were to be programmed, it is possible to violate the minimum of $\overline{RAS}$ precharge when $\overline{RAS}$ negates just before the beginning of T2.

To guarantee the precharge time, the DRAM controller will keep $\overline{DTACK}$ high for the 3 edges of precharge. $\overline{RAS}$ will assert from the 3rd positive edge of CLK, in either T4 or T5. To finish the delayed access, the DP8432V asserts $\overline{DTACK}$ after 2 clocks (one due to R2, R3 and one due to R6) on the positive edge of either T6 or T7. The 68040 will finish the access when it samples $\overline{TA}$ asserted at the end of either T7 or T8.

Burst Inhibited Cache Line Fill. Every time the 68040 addresses the DRAM array, SIZ0 and SIZ1 are decoded by the PAL. If these inputs are both 1s, the 68040 will do a line transfer (MOVE 16). In this case, the LineTx feedback will be driven high and $\overline{AREQ}$ and $\overline{ADS}$ will be held asserted. The input $\overline{TBI}$ to the 68040 is always asserted to indicate that there will be no burst access.

To continue cache filling, the 68040 finishes the opening access when it samples $\overline{TA}$ asserted at the end of T5 (rising edge of T1 second read). At this time, the 68040 increments the address bits A2 and A3 and asserts $\overline{TS}$ to continue with the second read. $\overline{HCAS}$ negates from the rising edge of

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clock (T1 2nd read) after $\overline{TA}$ asserts. $\overline{TS}$ low for the second read causes $\overline{HCAS}$ to assert from the rising edge of T2 (2nd read). $\overline{DTACK}$ is programmed to stay low during burst accesses (R4 = 0 R5 = 0). $\overline{HCAS}$ asserted from the rising edge of T2 causes $\overline{TA}$ to assert from the rising edge of T3. $\overline{TA}$ asserted allows the 68040 to latch the second piece of data. This logic allows 4 long word accesses to fill the cache line. During the 4th transfer TLN0 and TLN1 are both 1, driving LineTx high and $\overline{AREQ}$&$\overline{ADS}$ high. During the last three accesses of the cache fill, $\overline{TA}$ follows $\overline{HCAS}$ one CLK after.

Refresh Cycles. The DP8432V will automatically refresh a memory row every 15 μs. In the case where an access is in progress at the time of a refresh request, the DP8432V waits for the access to finish and precharge to take place before doing the refresh. In the same manner, if a refresh cycle is in progress and the 68040 request a memory access, the DP8432V will insert wait states into the CPU cycle to allow the refresh and precharge to finish. The DP8432V can insert a refresh cycle in between two back to back accesses.

Timing Analysis. Timing parameters starting with a "$" refer to the DP8430/31/32V-33 data sheet. Timing parameters starting with a "#" refer to the 68040 33 MHz data sheet. A 10 ns PAL with 8 ns delays on the registered outputs is used. The user can calculate new timings based on the equations given. This application note uses DRAMs with t_{RAC} = 80 ns, t_{CAC} = 20 ns and t_{AA} = 40 ns.

The AC timing parameters for the DRAM controller may have changed since this application note was written. The reader should refer to the latest data sheet.

$400b **$\overline{TS}$ Asserted Set Up to CLK High (8 ns min)**

= Tcp33 − Max PAL Delay to $\overline{ADS}$ and $\overline{AREQ}$ Asserted
= 30.3 − 8
= 22.3 ns

$401 **$\overline{CS}$ Asserted to $\overline{ADS}$ Asserted (2 ns min)**

= (Tcp + Min PAL Delay to $\overline{ADS}$ Asserted) − (#11 BCLK to Address Valid + Max Decoder Delay)
= (30.3 + 5.5) − (19 + 14)
= 35.8 − 33
= 2.8 ns

$404 **$407 Row/Bank Address Set Up to $\overline{ADS}$ Asserted (3 and 6 ns)**

= (Tcp + Min PAL Delay to $\overline{ADS}$ Asserted) − (#11 BCLK to Address Valid)
= 30.3 + 5.5 − 19
= 35.8 − 19
= 16.8 ns

#t6 **$\overline{TA}$ Set Up to BCLK High (8 ns min)**

Normal Access

= 1 Tcp33 − (Max PAL Delay to $\overline{TA}$ Asserted)
= 30.3 − 8
= 22.3 ns

Cache Filling Access (6 ns min)

= 1.0 Tcp33 − (Max PAL Delay to $\overline{TA}$ Asserted)
= 30.30 − 8
= 22.3 ns

t_{RAC} **Access Time from $\overline{RAS}$**

= 4Tcp33 − (Max PAL Delay to $\overline{ADS}$ Asserted + $402 $\overline{ADS}$ to $\overline{RAS}$ Asserted + #t15 Data Set Up Time)
= 121.2 − (8 + 20 + 5)
= 121.2 − 33
= 88.2 ns

t_{CAC} **Access Time from $\overline{CAS}$**

Normal Access (20 ns min)

= 4Tcp33 − (Max PAL Delay to $\overline{ADS}$ Asserted + $403 $\overline{ADS}$ to $\overline{CAS}$ Asserted + #t15 Data Set Up Time)
= 121.2 − (8 + 70 + 5)
= 121.2 − 83
= 38.2 ns

Cache Filling Access (20 ns min)

= 2Tcp33 − (Max PAL Delay to $\overline{HCAS}$ Asserted + Max OR Gate Delay + $14 Max $\overline{ECAS}$ Asserted to $\overline{CAS}$ Asserted + #t15 Data Set Up Time)
= 60.60 − (8 + 6 + 13 + 5)
= 60.60 − (32)
= 28.60 ns

t_{AA} **Access Time from Row Address Valid**

Normal Access (40 ns min)

= 4Tcp33 − (Max PAL Delay to $\overline{ADS}$ Asserted + $417 $\overline{ADS}$ to Row Address Valid + #t15 Data Set Up Time)

= 121.2 − (8 + 63 + 5)

= 121.2 − 76

= 45.2 ns

Cache Filling Access (40 ns min)

= 3Tcp33 − (#11 BCLK High to Address Valid + $26 Address Valid to Q Valid + #t15 Data Set Up Time)

= 90.90 − (19 + 20 + 5)

= 90.90 − 44

= 46.90 ns

t_{RP} **$\overline{RAS}$ Precharge (60 ns min)**

$\overline{RAS}$ Negates before the Positive Edge of T2. Typical Case.

= 3Tcp − (PAL Delay to $\overline{ADS}$ and $\overline{AREQ}$ negated + $13 $\overline{AREQ}$ to $\overline{RAS}$ negated)

= 90.90 − (6 ns + 20 ns)

= 64.90 ns

$\overline{RAS}$ Negates after the Positive Edge of T2.

= 4Tcp − Max (PAL Delay to $\overline{ADS}$ and $\overline{AREQ}$ Negated + $13 $\overline{AREQ}$ to $\overline{RAS}$ Negated)

= 121.20 − (8 + 25)

= 88.20 ns

3Ts of precharge must be programmed. 2Ts do not provide enough precharge time in the case where $\overline{RAS}$ negates just before T2.

t_{RAS} **$\overline{RAS}$ Refresh**

Refresh is programmed for 4Ts. Only choice with 3Ts of precharge.

PAL EQUATIONS

A PAL16R6 is used. Combinatorial outputs have a maximum propagation delay of 10 ns, registered outputs have a maximum propagation delay of 8 ns. The following PAL equations are used.

Inputs: BCLK, $\overline{RESET}$, $\overline{TS}$, TLN0, TLN1, SIZ0, SIZ1, $\overline{DTACK}$, $\overline{WE}$

Outputs: $\overline{AREQ}$, $\overline{TA}$, $\overline{HCAS}$, LineTx, $\overline{ML}$.

$\overline{AREQ}\sim\ := \overline{TS}\_\_ * RESET\_\_$
$\quad + \overline{AREQ}\_\_ * TA\_\_ * RESET\_\_$
$\quad + \overline{AREQ}\_\_ * LineTx * RESET\_\_$

$\overline{HCAS}\sim\ := \overline{TS}\_\_ * RESET\_\_$
$\quad + \overline{HCAS}\_\_ * TA\_\_ * RESET\_\_$

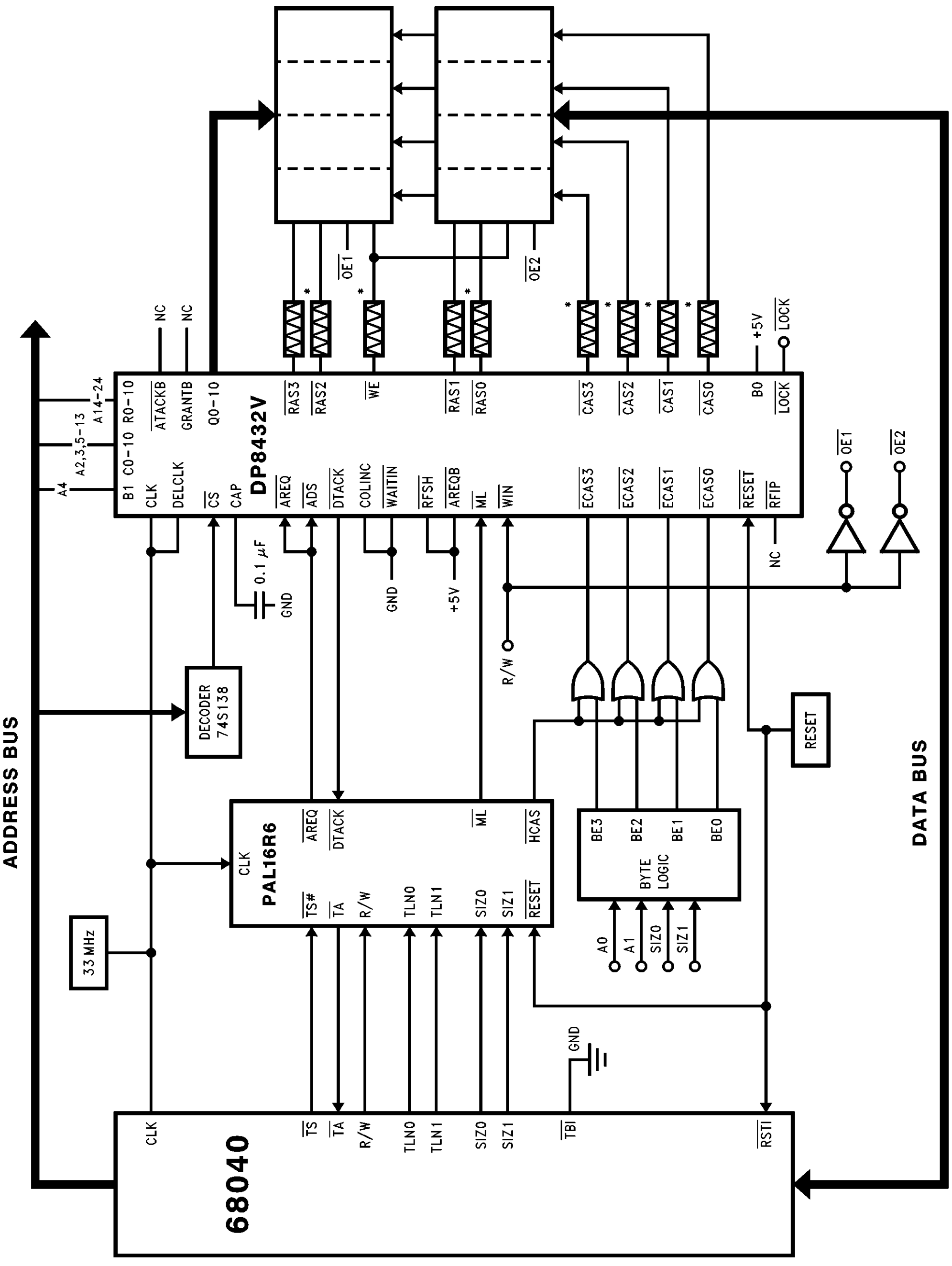
$\overline{TA}\sim\ := \overline{HCAS}\_\_ * \overline{DTACK}\_\_$

$LineTx\ = SIZ0 * \overline{TS}\_\_ * WE\_\_$
$\quad + LineTx * \overline{TLN0} * \overline{TLN1}$
$\quad + LineTx * TLN0 * \overline{TLN1}$
$\quad + LineTx * \overline{TLN0} * TLN1$

$\overline{ML}\sim\ := \overline{RESET}$
$\quad + \overline{ML}\_\_ * RESET\_\_ * \overline{WE}\_\_$
$\quad + \overline{ML}\_\_ * RESET\_\_ * TS\_\_$

DRAM CONTROLLER PROGRAMMING BITS:

$\overline{ECAS}$ = 0	C4 = 0	R6 = 0
B1 = 1	C3 = 0	R5 = 0
B2 = 1	C2 = 0	R4 = 0
C9 = 0	C1 = 1	R3 = 0
C8 = 1	C0 = 0	R2 = 1
C7 = 1	R9 = 0	R1 = 1
C6 = 1	R8 = 1	R0 = 1
C5 = 0	R7 = 1	



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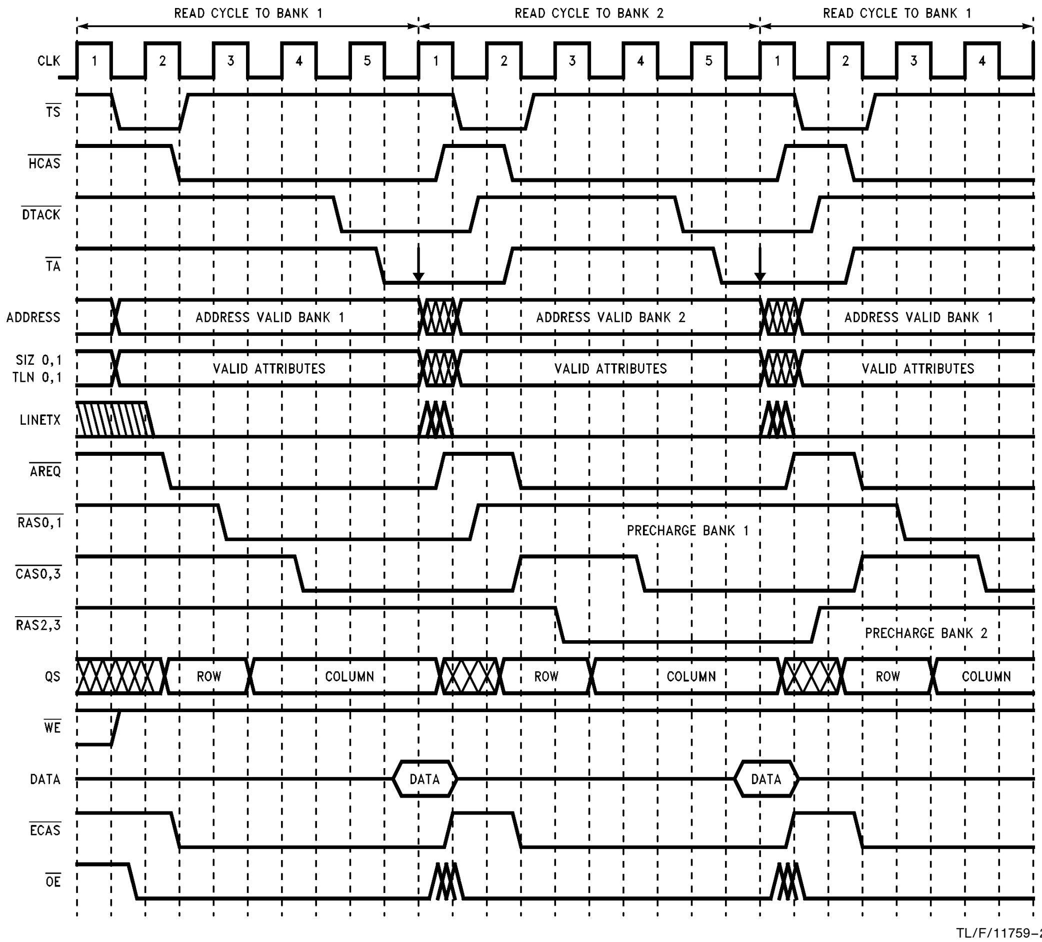
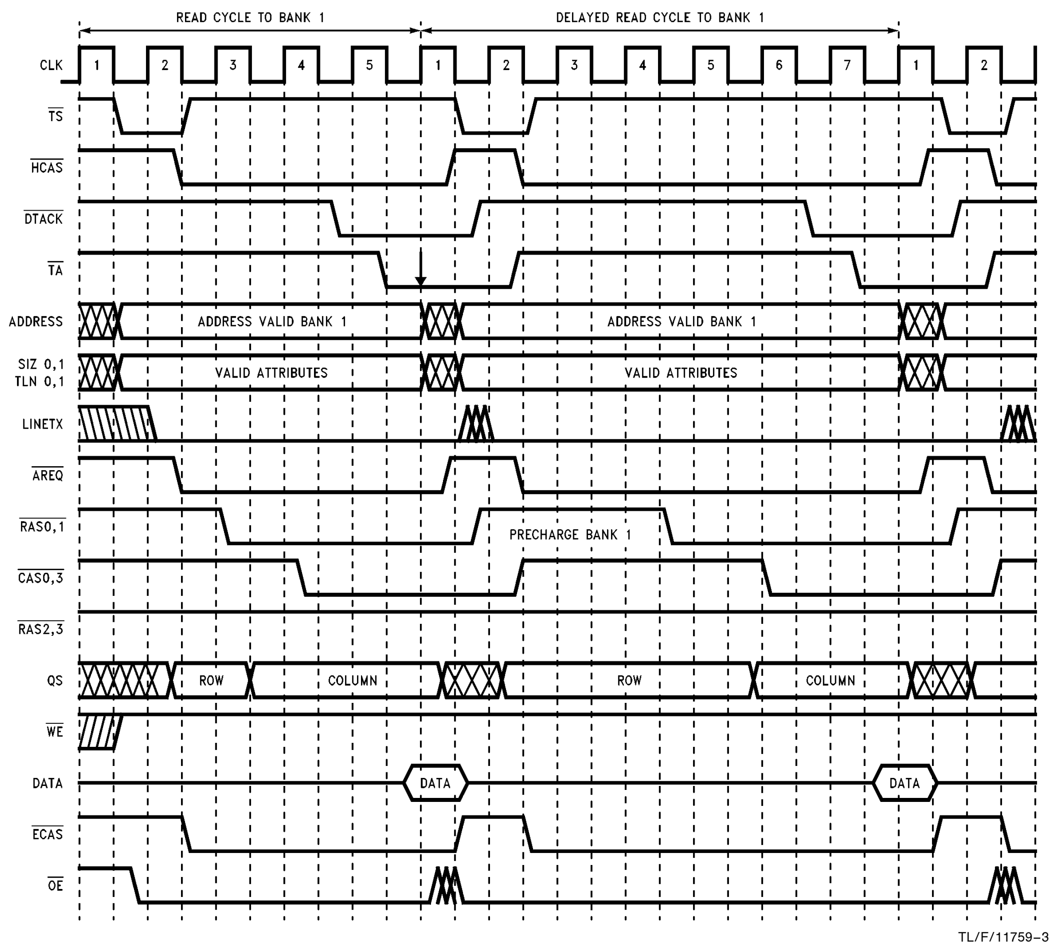
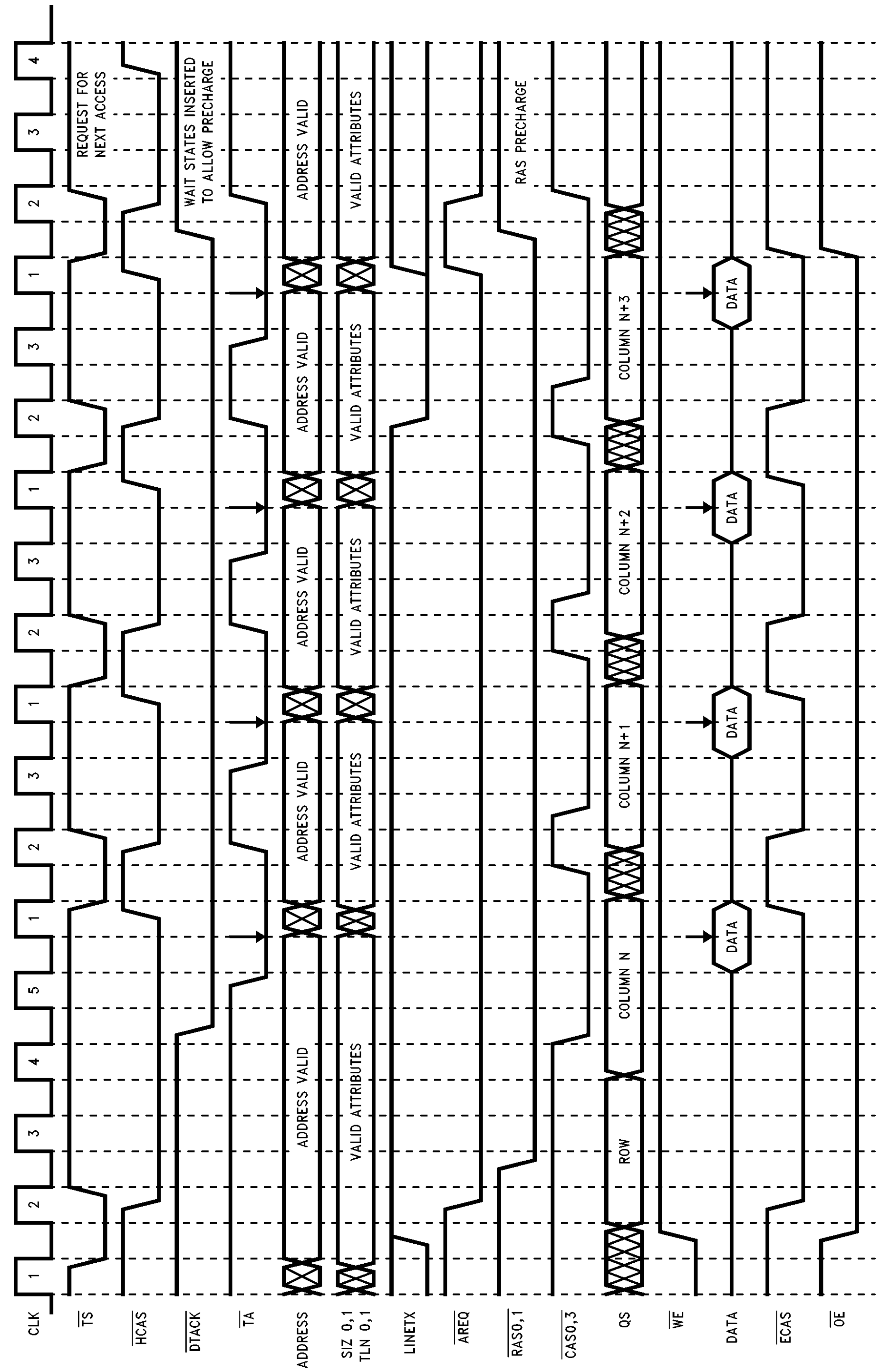
*Series damping resistors may not be needed.



Non Delayed Back to Back Access to Different Banks



Delayed Back to Back Access to Different Banks



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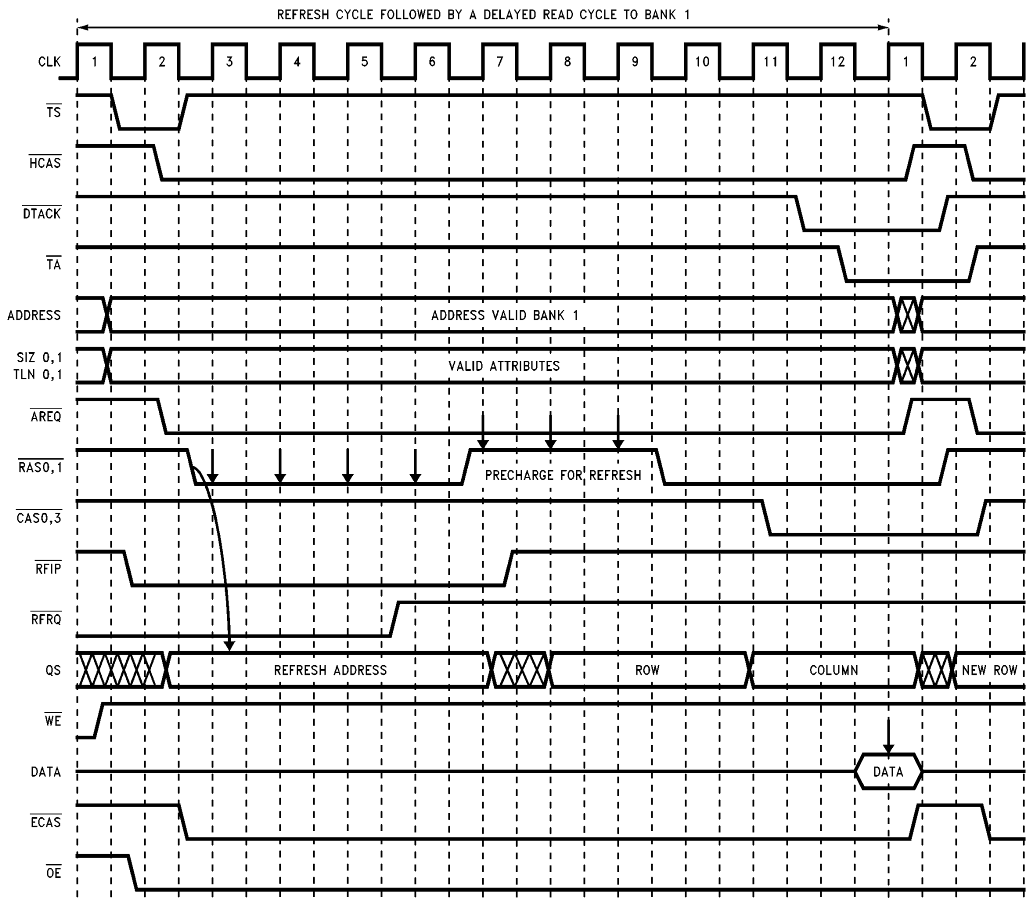
Burst Inhibited Cache Line Fill. 5-3-3-3



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Refresh Follow by an Access to Bank 1

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